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COPY

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Gonzalez *et al.*

Patent No.: 7,749,860 B2

Issued: July 6, 2010

For: METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH

Attorney Docket No.: 2269-6981.2US
(1996-0723.02/US)

Express Mail Mailing Label No.: EM 417186702 US

Date of Deposit with USPS: August 30, 2010

Person making Deposit: Grady Evans

REQUEST FOR CERTIFICATE OF CORRECTION FOR APPLICANTS' MISTAKES (37 C.F.R. § 1.323) AND PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)

Certificate

SEP 0 3 2010

of Correction

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following remarks are submitted with a Certificate of Correction filed herewith.

It is noted that a combination of Applicants' errors and Patent Office errors appear in this patent of a typographical or clerical nature or character. It is respectfully submitted that correction thereof does not involve such changes in the patent as would constitute new matter or would require reexamination. A certificate of correction in the form attached hereto is requested.

Please send the Certificate to:

Name: Katherine A. Hamer
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

09/02/2010 SZEWD1E1 00000019 7749860
01 FC:1811 100.00 OP

The amendments submitted herewith in the Certificate of Correction are submitted to correct the title of the patent and to correct the claims.

The title of the patent has been corrected by deleting the phrase "T-SHAPED."

In regard to the corrections to the claims, on November 23, 2009, Applicants filed an Amendment, which is referred to herein as the "November 23, 2009 Amendment." A copy of the November 23, 2009 Amendment is attached hereto as Exhibit A. On January 27, 2010, a Notice of Allowance was issued in this application in response to the November 23, 2009 Amendment.

On April 23, 2010, Applicants submitted an Amendment Pursuant to 37 C.F.R. §1.312(a) amending the specification and claims of this application, which is referred to herein as the Amendment Pursuant to 37 C.F.R. §1.312(a). A copy of the Amendment Pursuant to 37 C.F.R. §1.312(a) is attached hereto as Exhibit B. Due to a clerical error, the listing of claims included in the Amendment Pursuant to 37 C.F.R. §1.312(a) was incorrect because the claims did not include the amendments submitted in the November 23, 2009 Amendment. However, neither Applicants nor the Examiner noticed that the claims in the Amendment Pursuant to 37 C.F.R. §1.312(a) did not correspond to the amended claims presented in the November 23, 2009 Amendment, which were the claims allowed by the Examiner.

On June 3, 2010, the Examiner issued a Response to Rule 312 Communication indicating that the amendments under 37 C.F.R. §1.312(a) were entered as "to matters of form not affecting the scope of the invention."

The patent issued on July 6, 2010. A copy of the issued claims is attached hereto as Exhibit C. After reviewing the issued claims, Applicants noticed that the issued claims included a combination of language from the November 23, 2009 Amendment and the Amendment Pursuant to 37 C.F.R. §1.312(a) and, therefore, included Patent Office mistakes in addition to Applicants' mistakes.

The claim amendments submitted herewith in the Certificate of Correction are submitted to conform the issued claims (see Exhibit C) to the amended claims of the November 23, 2009 Amendment (see Exhibit A), which were the claims allowed by the Examiner. For the

Examiner's convenience, a clean copy of the claims, as to be amended by the Certificate of Correction, is attached hereto as Exhibit D.

The Commissioner is authorized to charge $100.00 to the TraskBritt Deposit Account No. 20-1469 for the fee as required by 37 C.F.R. § 1.20(a).

Attached hereto is Form PTO/SB/44, which is suitable for printing.

Respectfully submitted,

Katherine A. Hamer

Katherine A. Hamer
Registration No. 47,628
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: August 30, 2010
KAH/csw

Attachments: PTO/SB/44
Exhibit A: Copy of November 23, 2009 Amendment
Exhibit B: Copy of Amendment Pursuant to 37 C.F.R. §1.312(a)
Exhibit C: Copy of issued claims
Exhibit D: Copy of claims as amended by the Certificate of Correction

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,749,860 B2
APPLICATION NO. : 09/392,034
ISSUE DATE : July 6, 2010
INVENTOR(S) : Fernando Gonzalez, David Chapek, and Ranshir P. S. Thakur

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page:
In Item (54), change "**METHOD FOR FORMING A SELF-ALIGNED T-SHAPED ISOLATION TRENCH**" to **--METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH--**

In the specification:
COLUMN 1, LINE 2, delete "**T-SHAPED**"

In the claims:

CLAIM 1,	COLUMN 10,	LINE 59,	after "forming" insert --a first dielectric material upon-- and change "layer upon" to --over--
CLAIM 1,	COLUMN 10,	LINE 60,	delete "forming a first dielectric layer upon the oxide layer;"
CLAIM 1,	COLUMN 10,	LINE 61,	change "layer" to --material-- and after "expose" insert --a plurality of areas of--
CLAIM 1,	COLUMN 10,	LINE 62,	after "oxide" delete "layer at a plurality of areas"
CLAIM 1,	COLUMN 10,	LINE 63,	change "layer over the oxide layer and" to --material over--
CLAIM 1,	COLUMN 10,	LINES 64-66,	after "the first dielectric" delete "layer, wherein the forming a second dielectric layer includes forming a second dielectric layer over" and insert --material-- therefor
CLAIM 1,	COLUMN 10,	LINE 66,	after "with the" insert --plurality of--, after "exposed" insert --areas of the-- and after "oxide" delete "layer at"

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Katherine A. Hamer
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 1,	COLUMN 10,	LINE 67,	delete "the plurality of areas"
CLAIM 1,	COLUMN 11,	LINE 1,	change "layer" to --material--
CLAIM 1,	COLUMN 11,	LINE 2,	change "from the second dielectric layer," to --at peripheral edges of the plurality of exposed areas of--
CLAIM 1,	COLUMN 11,	LINE 3,	delete "wherein each spacer is situated upon" and delete "layer, is"
CLAIM 1,	COLUMN 11,	LINES 4-5,	after "contact with" insert --lateral edges of-- and delete "layer, and is adjacent to an area of the plurality of areas" and insert --material-- therefor
CLAIM 1,	COLUMN 11,	LINES 6-11,	change "forming a plurality of isolation trenches extending below the oxide layer into the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;" to --removing a portion of material from the plurality of areas of the oxide at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into the semiconductor substrate;--
CLAIM 1,	COLUMN 11,	LINE 12,	change "trench;" to --trench of the plurality of isolation trenches;--

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Katherine A. Hamer
TRASKBRITT
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Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 1,	COLUMN 11,	LINE 13,	delete "filling each isolation trench with" and insert therefor --implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;--, then insert --depositing-- before "a conformal," and change "layer" to --material in each isolation trench,--
CLAIM 1,	COLUMN 11,	LINE 14,	change "conformal layer" to --conformal material-- and change "above the oxide layer" to --over remaining portions of the oxide--
CLAIM 1,	COLUMN 11,	LINE 16,	change "filling" to --depositing-- and after "performed" delete "by depositing the conformal layer,"
CLAIM 1,	COLUMN 11,	LINE 17,	delete "and the depositing is carried out"
CLAIM 1,	COLUMN 11,	LINE 19,	change "layer" to --material--
CLAIM 1,	COLUMN 11,	LINE 20,	change "layer;" to --material;--
CLAIM 1,	COLUMN 11,	LINES 21-23,	change "substantially simultaneously subjecting the entire upper surface contour of" to --removing portions of--, change "layer to a planarizing process and" to --material overlying the remaining portions of the oxide by--, and change "layer" to --material--
CLAIM 1,	COLUMN 11,	LINES 24-25,	change "layer" to --material--, change "to form therefrom" to --such that--, and change "that is" to --is--

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TRASKBRITT
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 1,	COLUMN 11,	LINES 26-28,	change "surfaces; and" to --surfaces,--, delete the paragraph break, delete "fusing the oxide layer, liner, spacers, and conformal layer; wherein," and change "layer comprises" to --material comprising--
CLAIM 1,	COLUMN 11,	LINE 30,	change "trenches." to --trenches; and--, insert a paragraph break and then insert --removing the first dielectric material and portions of the oxide underlying the first dielectric material such that the conformal material fills each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal material start on an upper surface of the semiconductor substrate and are substantially orthogonal to the upper surface contour of the conformal material.--
CLAIM 4,	COLUMN 11,	LINE 37,	change "further comprising" to --wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide comprises--
CLAIM 4,	COLUMN 11,	LINE 38,	after "each" insert --of said plurality of--
CLAIM 4,	COLUMN 11,	LINE 39,	change "trench" to --trenches--

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TRASKBRITT
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Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 4,	COLUMN 11,	LINES 40-41,	change "the upper surface for each isolation trench is formed" to --removing portions of the conformal material overlying the remaining portions of the oxide comprises removing portions of the conformal material overlying the remaining portions of the oxide--
CLAIM 6,	COLUMN 11,	LINE 45,	change "dielectric layer" to --dielectric material-- and change "oxide layer" to --oxide--
CLAIM 6,	COLUMN 11,	LINE 47,	change "dielectric layer" to --dielectric material-- and after "expose" insert --a plurality of areas of--
CLAIM 6,	COLUMN 11,	LINE 48,	after "oxide" delete "layer at a plurality of areas"
CLAIM 6,	COLUMN 11,	LINE 49,	change "dielectric layer" to --dielectric material-- and after "over" delete "the oxide layer and"
CLAIM 6,	COLUMN 11,	LINES 50-53,	change "layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on" to --material--, change "exposed oxide layer at the plurality of" to --plurality of exposed-- and after "areas" insert --of the oxide--
CLAIM 6,	COLUMN 11,	LINE 54,	change "dielectric layer" to --dielectric material--
CLAIM 6,	COLUMN 11,	LINE 55,	change "from the second dielectric layer," to --at peripheral edges of the plurality of exposed areas of--
CLAIM 6,	COLUMN 11,	LINE 56,	delete "wherein each spacer is situated upon" and delete "layer, is"

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TRASKBRITT
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In the claims (continued):

CLAIM 6,	COLUMN 11,	LINES 57-58,	after "with" insert --lateral edges of-- and change "layer, and is adjacent to an area of the plurality of areas;" to --material;--
CLAIM 6,	COLUMN 11,	LINE 60,	change "forming" to --removing a portion of material from the plurality of areas of the oxide at locations between adjacent portions of the plurality of spacers to form-- and delete "below"
CLAIM 6,	COLUMN 11,	LINE 61,	delete "the oxide layer" and change "substrate," to --substrate;--
CLAIM 6,	COLUMN 11,	LINES 62-65,	delete "wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has an edge;"
CLAIM 6,	COLUMN 12,	LINE 1,	change "filling each isolation trench with" to --implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;--, then insert a paragraph break, insert --depositing-- before "a conformal" and change "layer," to --material filling each isolation trench,--
CLAIM 6,	COLUMN 12,	LINE 2,	change "layer" to --material--, change "above" to --over remaining portions of--, and after "oxide" delete "layer"
CLAIM 6,	COLUMN 12,	LINE 4,	change "filling is performed by" to --the-- and delete "the conformal layer"

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 6,	COLUMN 12,	LINE 5,	delete "and depositing"
CLAIM 6,	COLUMN 12,	LINE 7,	change "layer" to --material--
CLAIM 6,	COLUMN 12,	LINE 8,	change "layer;" to --material;--
CLAIM 6,	COLUMN 12,	LINES 9-10,	change "substantially simultaneously subjecting an entire upper surface contour" to --removing portions-- and change "layer to a" to --material that overlie the remaining portions of the oxide by--
CLAIM 6,	COLUMN 12,	LINE 11,	delete "process and planarizing" and change "layer" to --material--
CLAIM 6,	COLUMN 12,	LINE 12,	delete "therefrom"
CLAIM 6,	COLUMN 12,	LINE 14,	delete "fusing the oxide layer, spacers and conformal layer;"
CLAIM 6,	COLUMN 12,	LINE 15,	before "wherein" insert --removing the first dielectric material and portions of the oxide underlying the first dielectric material such that the conformal material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal material begin on an upper surface of the semiconductor substrate and are oriented substantially orthogonal to the upper surface contour of the conformal material--
CLAIM 6,	COLUMN 12,	LINE 16,	change "layer comprises a material that" to --material--
CLAIM 6,	COLUMN 12,	LINE 19,	change "layer" to --material--
CLAIM 6,	COLUMN 12,	LINE 21,	change "layer" to --material--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 6,	COLUMN 12,	LINE 22,	change "oxide layer; and" to --oxide; and--
CLAIM 6,	COLUMN 12,	LINE 23,	change "layer" to --material—
CLAIM 6,	COLUMN 12,	LINE 24,	change "oxide layer." to --oxide.--
CLAIM 9,	COLUMN 12,	LINE 36,	change "material the ratio is" to --material using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio-- and change "from about" to --of from about--
CLAIM 10,	COLUMN 12,	LINE 38,	change "overlying" to --that overlie--
CLAIM 13,	COLUMN 12,	LINE 61,	change "oxide layer" to --oxide--
CLAIM 13,	COLUMN 12,	LINE 62,	change "nitride layer" to --nitride-- and change "oxide layer;" to --oxide;--
CLAIM 13,	COLUMN 12,	LINE 63,	change "nitride layer" to --nitride-- and after "expose" insert --a plurality of areas of--
CLAIM 13,	COLUMN 12,	LINE 64,	change "oxide layer at a plurality of areas;" to --oxide;--
CLAIM 13,	COLUMN 12,	LINE 65,	change "layer over the oxide layer" to --material over--
CLAIM 13,	COLUMN 12,	LINE 66,	delete "and over," and delete "layer, wherein forming a first"
CLAIM 13,	COLUMN 12,	LINE 67,	delete "silicon dioxide layer includes forming a first silicon"
CLAIM 13,	COLUMN 13,	LINE 1,	delete "dioxide layer on" and change "the exposed oxide" to --the plurality of exposed areas of the oxide;--
CLAIM 13,	COLUMN 13,	LINE 2,	delete "layer at the plurality of areas;"
CLAIM 13,	COLUMN 13,	LINE 3,	change "layer" to --material--

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TRASKBRITT
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 13, COLUMN 13, LINE 4,	change "from the first silicon dioxide layer," to --at the peripheral edges of the plurality of exposed areas of--
CLAIM 13, COLUMN 13, LINE 5,	delete "wherein each spacer is situated upon" and delete "layer, is"
CLAIM 13, COLUMN 13, LINES 6-7,	change "silicon nitride layer, and is adjacent to an area of the plurality of areas;" to --lateral edges of the silicon nitride;--
CLAIM 13, COLUMN 13, LINE 8,	change "forming" to --removing a portion of material from the plurality of areas at locations between adjacent portions of the plurality of spacers to form-- and change "below" to --into--
CLAIM 13, COLUMN 13, LINE 9,	delete "the oxide layer into and terminating within"
CLAIM 13, COLUMN 13, LINES 10-13,	change "substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;" to --substrate;--
CLAIM 13, COLUMN 13, LINES 17-21,	change "trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer to the termination of the isolation trench within the semiconductor substrate;" to --trench;--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 13, COLUMN 13, LINE 22,	change "filling each isolation trench with" to --implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;--, insert a paragraph break, and then insert --depositing--
CLAIM 13, COLUMN 13, LINE 23,	change "layer, the conformal second silicon dioxide" to --material filling--
CLAIM 13, COLUMN 13, LINE 24,	delete "layer within" and change "trench extending above" to --trench, the conformal second silicon dioxide material within each isolation trench and extending over remaining portions of--
CLAIM 13, COLUMN 13, LINE 25,	delete "layer"
CLAIM 13, COLUMN 13, LINE 26,	change "wherein filling is performed by depositing the" to --the--
CLAIM 13, COLUMN 13, LINE 27,	delete "conformal second silicon dioxide layer, and"
CLAIM 13, COLUMN 13, LINE 30,	delete "layer"
CLAIM 13, COLUMN 13, LINE 31,	change "dioxide layer;" to --dioxide material;--
CLAIM 13, COLUMN 13, LINE 32,	delete "substantially simultaneously subjecting an entire upper"
CLAIM 13, COLUMN 13, LINE 33,	change "surface contour" to --removing portions--
CLAIM 13, COLUMN 13, LINE 34,	change "layer to a" to --material by-- and delete "process so as to remove"
CLAIM 13, COLUMN 13, LINE 35,	change "dioxide layer" to --dioxide material--

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TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 13,	COLUMN 13, LINE 37,	change "surfaces and being situated" to --surfaces,--
CLAIM 13,	COLUMN 13, LINE 38,	delete "above the oxide layer," and change "a material that is" to --an--
CLAIM 13,	COLUMN 13, LINE 39,	after "insulative" insert --material--
CLAIM 13,	COLUMN 13, LINES 41-42,	change "fusing the oxide layer, liner, spacers, and conformal second silicon dioxide layer." to -- removing the silicon nitride and portions of the oxide underlying the silicon nitride such that the conformal second silicon dioxide material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second silicon dioxide material start on an upper surface of the semiconductor substrate and lie substantially orthogonal to the upper surface contour of the second silicon dioxide material.--
CLAIM 17,	COLUMN 13, LINE 54,	change "oxide layer" to --oxide--
CLAIM 17,	COLUMN 13, LINE 55,	change "a polysilicon layer" to --polysilicon-- and change "oxide layer;" to --oxide;--
CLAIM 17,	COLUMN 13, LINE 56,	change "dielectric layer" to --dielectric material-- and change "polysilicon layer;" to --polysilicon;--
CLAIM 17,	COLUMN 13, LINE 57,	change "dielectric layer" to --dielectric material--
CLAIM 17,	COLUMN 13, LINES 58-59,	change "layer to expose" to --to expose-- and after "expose" insert --a plurality of areas of-- and change "oxide layer at a plurality of areas;" to --oxide;--

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Katherine A. Hamer
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,749,860 B2
APPLICATION NO. : 09/392,034
ISSUE DATE : July 6, 2010
INVENTOR(S) : Fernando Gonzalez, David Chapek, and Ranshir P. S. Thakur

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 17,	COLUMN 13, LINE 60,	change "dielectric layer" to --dielectric material--
CLAIM 17,	COLUMN 13, LINE 61,	change "oxide layer, the polysilicon layer, and" to --polysilicon,--
CLAIM 17,	COLUMN 13, LINES 62-65,	change "layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;" to --material and in contact with the plurality of exposed areas of the oxide;--
CLAIM 17,	COLUMN 13, LINE 66,	change "dielectric layer" to --dielectric material--
CLAIM 17,	COLUMN 13, LINE 67,	change "from the second dielectric layer," to --at peripheral edges of the plurality of exposed areas of the oxide--
CLAIM 17,	COLUMN 14, LINE 1,	delete "wherein each spacer is upon the oxide layer, is"
CLAIM 17,	COLUMN 14, LINE 2,	change "both the polysilicon layer and" to --lateral edges of--
CLAIM 17,	COLUMN 14, LINE 3,	change "layer, and is adjacent to an area of the plurality of areas;" to --material;--
CLAIM 17,	COLUMN 14, LINE 4,	change "forming" to --removing a portion of material from the plurality of areas of the oxide at locations between adjacent portions of the plurality of spacers to form-- and delete "below"
CLAIM 17,	COLUMN 14, LINE 5,	delete "the oxide layer and from top edges"

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TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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INVENTOR(S) : Fernando Gonzalez, David Chapek, and Ranshir P. S. Thakur

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 17, COLUMN 14,	LINES 6-9,	change "substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;" to --substrate;--
CLAIM 17, COLUMN 14,	LINE 11,	before "filling" insert --implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;--, insert a paragraph break, insert --depositing a conformal third material--, and delete "with a conformal third layer,"
CLAIM 17, COLUMN 14,	LINE 12,	change "layer extending above" to --material extending over remaining portions of--
CLAIM 17, COLUMN 14,	LINE 13,	delete "layer"
CLAIM 17, COLUMN 14,	LINE 14,	delete "filling is performed by depositing the conformal"
CLAIM 17, COLUMN 14,	LINE 15,	delete "third layer, and"
CLAIM 17, COLUMN 14,	LINE 17,	change "dielectric layer" to --dielectric material--
CLAIM 17, COLUMN 14,	LINE 18,	change "third layer;" to --third material;--
CLAIM 17, COLUMN 14,	LINES 19-20,	change "substantially simultaneously subjecting an entire upper surface contour" to --removing portions-- and change "layer to a" to --material by--
CLAIM 17, COLUMN 14,	LINE 21,	delete "process and planarizing"
CLAIM 17, COLUMN 14,	LINE 22,	change "layer" to --material-- and delete "therefrom"

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TRASKBRITT
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INVENTOR(S) : Fernando Gonzalez, David Chapek, and Ranshir P. S. Thakur

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 17, COLUMN 14, LINE 25,	change "fusing the oxide layer, spacers and conformal third layer;" to -- removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material;--
CLAIM 17, COLUMN 14, LINE 30,	change "third layer," to --third material,--
CLAIM 18, COLUMN 14, LINES 32-33,	change "the upper surface for each isolation trench is formed" to --removing portions of the conformal third material comprises removing portions of the conformal third material--
CLAIM 22, COLUMN 14, LINE 52,	change "oxide layer" to --oxide--
CLAIM 22, COLUMN 14, LINE 53,	change "a polysilicon layer" to --polysilicon-- and change "oxide layer;" to --oxide;--
CLAIM 22, COLUMN 14, LINE 54,	change "dielectric layer" to --dielectric material-- and change "polysilicon layer;" to --polysilicon;--

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Salt Lake City, Utah 84102 USA

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INVENTOR(S) : Fernando Gonzalez, David Chapek, and Ranshir P. S. Thakur

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 22, COLUMN 14,	LINES 55-57,	change "dielectric layer" to --dielectric material--, change "polysilicon layer" to --polysilicon--, and change "expose the oxide layer at a plurality of areas;" to --expose a plurality of areas of the oxide;--
CLAIM 22, COLUMN 14,	LINE 58,	change "dielectric layer conformally" to --dielectric material--
CLAIM 22, COLUMN 14,	LINE 59,	delete "oxide layer, the" and change "polysilicon layer, and" to --polysilicon,--
CLAIM 22, COLUMN 14,	LINES 60-62,	change "layer, wherein forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;" to --material and in contact with the plurality of exposed areas of the oxide;--
CLAIM 22, COLUMN 14,	LINE 63,	change "dielectric layer" to --dielectric material--
CLAIM 22, COLUMN 14,	LINE 64,	change "from the second dielectric layer," to --at the peripheral edges of the plurality of exposed areas of--
CLAIM 22, COLUMN 14,	LINE 65,	change "wherein each spacer is upon the oxide layer, is" to --the oxide--
CLAIM 22, COLUMN 14,	LINE 66,	change "both the polysilicon layer and" to --lateral edges of--
CLAIM 22, COLUMN 14,	LINE 67,	change "layer, and is adjacent to an area of the plurality of areas;" to --material;--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 22, COLUMN 15, LINE 1,	change "forming" to --removing a portion of material from the plurality of exposed areas of the oxide at locations between adjacent portions of the plurality of spacers to form-- and delete "below"
CLAIM 22, COLUMN 15, LINE 2,	delete "the oxide layer and from top edges"
CLAIM 22, COLUMN 15, LINES 3-6,	change "substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;" to --substrate;--
CLAIM 22, COLUMN 15, LINES 7-8,	change "rounding the top edges of each isolation trench of the plurality of isolation trenches;" to --implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;--
CLAIM 22, COLUMN 15, LINES 9-10,	change "filling each isolation trench of the plurality of isolation trenches with" to --depositing-- and change "layer," to --material filling each isolation trench,--
CLAIM 22, COLUMN 15, LINE 11,	change "third layer" to --third material-- and change "above the oxide layer" to --over remaining portions of the oxide--
CLAIM 22, COLUMN 15, LINE 12,	delete "filling"
CLAIM 22, COLUMN 15, LINE 13,	delete "is performed by depositing the conformal third layer,"
CLAIM 22, COLUMN 15, LINE 14,	delete "and"

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 22, COLUMN 15, LINE 16,	change "dielectric layer" to --dielectric material--
CLAIM 22, COLUMN 15, LINE 17,	change "third layer;" to ----third material;--
CLAIM 22, COLUMN 15, LINE 18,	delete "substantially simultaneously subjecting an entire upper"
CLAIM 22, COLUMN 15, LINE 19,	change "surface contour" to --removing portions-- and change "third layer to a" to --third material by--
CLAIM 22, COLUMN 15, LINE 20,	delete "process and planarizing"
CLAIM 22, COLUMN 15, LINE 21,	change "layer" to --material-- and delete "therefrom"
CLAIM 22, COLUMN 15, LINES 23-24,	insert a paragraph break after "and" and then change "fusing the oxide layer, spacers and conformal third layer;" to -- removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material;--
CLAIM 22, COLUMN 15, LINE 25,	change "third layer is an" to --third material is--
CLAIM 22, COLUMN 15, LINE 26,	change "material that" to --and--

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TRASKBRITT
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 22, COLUMN 15,	LINE 30,	change "third layer," to --third material,--
CLAIM 22, COLUMN 15,	LINE 31,	change "layer; and" to --material; and--
CLAIM 22, COLUMN 15,	LINE 33,	change "third layer," to --third material,--
CLAIM 23, COLUMN 15,	LINE 37,	change "oxide layer" to --oxide--
CLAIM 23, COLUMN 15,	LINE 38,	change "polysilicon layer" to --first polysilicon material-- and change "oxide layer;" to --oxide;--
CLAIM 23, COLUMN 15,	LINE 39,	change "dielectric layer" to --dielectric material-- and change "polysilicon layer;" to --first polysilicon material;--
CLAIM 23, COLUMN 15,	LINE 40,	change "dielectric layer" to --dielectric material-- and after "and the" insert --first--
CLAIM 23, COLUMN 15,	LINES 41-42,	change "layer to expose the oxide layer at a plurality of areas;" to --material to expose a plurality of areas of the oxide;--
CLAIM 23, COLUMN 15,	LINE 43,	change "dielectric layer conformally" to --dielectric material--
CLAIM 23, COLUMN 15,	LINE 44,	delete "oxide layer, the polysilicon layer, and the"
CLAIM 23, COLUMN 15,	LINE 45,	delete "layer, wherein the forming a second dielectric layer"
CLAIM 23, COLUMN 15,	LINE 46,	change "includes forming a second dielectric layer on" to --material--
CLAIM 23, COLUMN 15,	LINES 47-48,	after "with the" insert --plurality of-- and change "oxide layer at the plurality of areas;" to --areas of the oxide;--

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Katherine A. Hamer
TRASKBRITT
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Salt Lake City, Utah 84102 USA

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INVENTOR(S) : Fernando Gonzalez, David Chapek, and Ranshir P. S. Thakur

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 23, COLUMN 15, LINE 49,	change "dielectric layer" to --dielectric material--
CLAIM 23, COLUMN 15, LINE 50,	change "from the second dielectric layer," to --at peripheral edges of the plurality of exposed areas of--
CLAIM 23, COLUMN 15, LINE 51,	delete "wherein each spacer of the plurality of spacers is upon"
CLAIM 23, COLUMN 15, LINE 52,	change "oxide layer, is" to --oxide in-- and change "both the polysilicon" to --lateral edges of--
CLAIM 23, COLUMN 15, LINES 53-54,	delete "layer and" and change "dielectric layer, and is adjacent to an area of the plurality of areas;" to --dielectric material;--
CLAIM 23, COLUMN 15, LINE 55,	change "forming" to --removing a portion of material from the plurality of exposed areas of the oxide at locations between adjacent portions of the plurality of spacers to form-- and delete "below"
CLAIM 23, COLUMN 15, LINE 56,	delete "the oxide layer and from top edges"
CLAIM 23, COLUMN 15, LINES 57-60,	change "substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;" to --substrate;--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 23,	COLUMN 15,	LINE 62, before "filling" insert --implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;--, insert a paragraph break, and then insert --depositing a conformal third material-- and change "trench with a conformal third layer," to --trench,--
CLAIM 23,	COLUMN 15,	LINE 63, change "third layer extending above" to --third material extending over remaining portions of--
CLAIM 23,	COLUMN 15,	LINE 64, delete "layer"
CLAIM 23,	COLUMN 15,	LINE 65, delete "filling is performed by depositing the conformal"
CLAIM 23,	COLUMN 15,	LINE 66, delete "third layer, and"
CLAIM 23,	COLUMN 16,	LINE 1, change "dielectric layer" to --dielectric material--
CLAIM 23,	COLUMN 16,	LINE 2, change "third layer;" to --third material;--
CLAIM 23,	COLUMN 16,	LINE 3, delete "substantially simultaneously subjecting an entire upper"
CLAIM 23,	COLUMN 16,	LINE 4, change "surface contour" to --removing portions-- and change "third layer to a" to --third material overlying the remaining portions of the oxide by--
CLAIM 23,	COLUMN 16,	LINE 5, delete "process and planarizing"
CLAIM 23,	COLUMN 16,	LINE 6, change "layer" to --material-- and delete "therefrom"
CLAIM 23,	COLUMN 16,	LINE 8, change "oxide layer" to --oxide--
CLAIM 23,	COLUMN 16,	LINE 10, change "oxide layer" to --oxide--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 23, COLUMN 16, LINE 13,	change "layer composed of" to --second--
CLAIM 23, COLUMN 16, LINE 14,	after "polysilicon" insert --material-- and delete "layer"
CLAIM 23, COLUMN 16, LINE 16,	change "third layer," to --conformal third material,--
CLAIM 23, COLUMN 16, LINE 17,	change "layer composed of polysilicon" to --second polysilicon material--
CLAIM 23, COLUMN 16, LINE 19,	change "fusing the oxide layer, spacers and conformal third layer;" to -- removing the first dielectric material, first polysilicon material and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate and extend to the upper surface contour of the conformal third material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material;--
CLAIM 24, COLUMN 16, LINE 25,	delete "forming an oxide layer upon a semiconductor substrate;"
CLAIM 24, COLUMN 16, LINE 26,	change "a polysilicon layer" to --polysilicon-- and change "the oxide layer;" to --an oxide overlying a semiconductor substrate;--

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TRASKBRITT
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 24,	COLUMN 16, LINE 27,	change "dielectric layer" to --dielectric material-- and change "polysilicon layer;" to --polysilicon;--
CLAIM 24,	COLUMN 16, LINE 28,	change "dielectric layer" to --dielectric material--
CLAIM 24,	COLUMN 16, LINE 29,	change "layer to expose the oxide layer at a plurality of" to --to expose a plurality of areas of the oxide;--
CLAIM 24,	COLUMN 16, LINE 30,	delete "areas;"
CLAIM 24,	COLUMN 16, LINE 31,	change "dielectric layer conformally" to --dielectric material--
CLAIM 24,	COLUMN 16, LINE 32,	change "oxide layer, the polysilicon layer," to --polysilicon,--
CLAIM 24,	COLUMN 16, LINE 33,	change "layer, wherein the forming a second dielectric layer" to --material--
CLAIM 24,	COLUMN 16, LINE 34,	delete "includes forming a second dielectric layer on"
CLAIM 24,	COLUMN 16, LINE 35,	after "with the" insert --plurality of-- and change "oxide layer at the plurality of" to --areas of the oxide;--
CLAIM 24,	COLUMN 16, LINE 36,	delete "areas;"
CLAIM 24,	COLUMN 16, LINE 37,	change "dielectric layer" to --dielectric material--
CLAIM 24,	COLUMN 16, LINE 38,	change "from the second dielectric layer," to --at peripheral edges of the plurality of exposed areas of--
CLAIM 24,	COLUMN 16, LINE 39,	delete "wherein each spacer of the plurality of spacers is upon"
CLAIM 24,	COLUMN 16, LINE 40,	delete "layer, is" and change "both the polysilicon" to --lateral edges of--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 24, COLUMN 16, LINE 41,	delete "layer and" and change "layer, and is adjacent to an" to --material;--
CLAIM 24, COLUMN 16, LINE 42,	delete "area of the plurality of areas;"
CLAIM 24, COLUMN 16, LINE 43,	change "forming" to --removing material from the plurality of exposed areas of the oxide at locations between adjacent portions of the plurality of spacers to form-- and delete "below"
CLAIM 24, COLUMN 16, LINE 44,	delete "the oxide layer and from top edges"
CLAIM 24, COLUMN 16, LINES 45-48,	change "substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;" to --substrate;--
CLAIM 24, COLUMN 16, LINE 50,	after "trenches;" insert a paragraph break and then insert -- implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;--
CLAIM 24, COLUMN 16, LINE 51,	before "filling" insert --depositing a conformal third material-- and change "trench with a conformal third layer," to --trench,--
CLAIM 24, COLUMN 16, LINE 52,	change "third layer extending above" to --third material extending over remaining portions of--
CLAIM 24, COLUMN 16, LINE 53,	change "layer in" to --in--
CLAIM 24, COLUMN 16, LINE 54,	delete "filling is performed by depositing the conformal"

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 24,	COLUMN 16, LINE 55,	delete "third layer, and"
CLAIM 24,	COLUMN 16, LINE 57,	change "dielectric layer" to --dielectric material--
CLAIM 24,	COLUMN 16, LINE 58,	change "third layer;" to --third material;--
CLAIM 24,	COLUMN 16, LINE 59,	delete "substantially simultaneously subjecting an entire upper"
CLAIM 24,	COLUMN 16, LINE 60,	change "surface contour" to --removing portions-- and change "layer to a" to --material overlying the remaining portions of the oxide by--
CLAIM 24,	COLUMN 16, LINE 61,	change "process comprising" to --the conformal third material to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces using--
CLAIM 24,	COLUMN 16, LINE 62,	change "third layer" to --third material--
CLAIM 24,	COLUMN 16, LINE 63,	change "dielectric" to --dielectric material-- and change "range from" to --range of from--
CLAIM 24,	COLUMN 16, LINES 64-66,	change "2:1 and planarizing the conformal third layer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces; and" to --2:1;--

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Katherine A. Hamer
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,749,860 B2
APPLICATION NO. : 09/392,034
ISSUE DATE : July 6, 2010
INVENTOR(S) : Fernando Gonzalez, David Chapek, and Ranshir P. S. Thakur

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 24, COLUMN 16, LINE 67,	change "fusing the oxide layer," to --heat treating the oxide,-- change "third layer;" to --third material to fuse the oxide, spacers and conformal third material; and--, insert a paragraph break and then insert --removing the first dielectric material, polysilicon, and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material;--
CLAIM 24, COLUMN 17, LINE 5,	change "third layer," to --third material,--
CLAIM 24, COLUMN 17, LINES 6-11,	delete "corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric material so as to define an upper surface contour of the conformal third material;"
CLAIM 26, COLUMN 17, LINE 16,	change "oxide layer" to --oxide--
CLAIM 26, COLUMN 17, LINE 17,	change "polysilicon layer" to --first polysilicon material-- and change "oxide layer;" to --oxide;--

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TRASKBRITT
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Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 26,	COLUMN 17, LINE 18,	change "a silicon nitride layer" to --silicon nitride-- and change "polysilicon layer;" to --first polysilicon material;--
CLAIM 26,	COLUMN 17, LINE 19,	change "layer and the" to --and the first--
CLAIM 26,	COLUMN 17, LINE 20,	change "layer to expose" to --material to expose a plurality of areas of-- and change "layer at a plurality" to --material;--
CLAIM 26,	COLUMN 17, LINE 21,	delete "of areas;"
CLAIM 26,	COLUMN 17, LINE 22,	change "layer over the pad oxide" to --material over--
CLAIM 26,	COLUMN 17, LINES 23-25,	delete "layer and over" and delete "layer, wherein the forming a first silicon dioxide layer includes forming a first silicon dioxide layer on"
CLAIM 26,	COLUMN 17, LINE 26,	delete "layer" and change "areas;" to --exposed areas of the pad oxide;--
CLAIM 26,	COLUMN 17, LINE 27,	change "dioxide layer" to --dioxide material--
CLAIM 26,	COLUMN 17, LINES 28-29,	change "from the first silicon dioxide layer, wherein each spacer of the plurality of spacers is situated" to --at peripheral edges of the plurality of exposed areas of--
CLAIM 26,	COLUMN 17, LINE 30,	delete "upon," delete "layer, is" and after "with" insert --lateral edges of--
CLAIM 26,	COLUMN 17, LINE 31,	change "nitride layer and the polysilicon layer, and is adjacent to" to --nitride and the first polysilicon material;--

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TRASKBRITT
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Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 26, COLUMN 17, LINE 32,	delete "an area of the plurality of areas;"
CLAIM 26, COLUMN 17, LINE 33,	change "forming" to --removing a portion of material from the plurality of exposed areas at locations between adjacent portions of the plurality of spacers to form-- and delete "below"
CLAIM 26, COLUMN 17, LINE 34,	delete "the pad oxide layer and from top edges"
CLAIM 26, COLUMN 17, LINE 41,	change "substrate;" to --substrate by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the pad oxide;--
CLAIM 26, COLUMN 17, LINE 44,	delete "layer"
CLAIM 26, COLUMN 17, LINE 47,	before "filling" insert --depositing a conformal second material-- and delete "with a conformal second layer,"
CLAIM 26, COLUMN 17, LINE 48,	change "layer extending above" to --material extending over remaining portions of--
CLAIM 26, COLUMN 17, LINE 49,	delete "layer"
CLAIM 26, COLUMN 17, LINE 50,	delete "filling is performed by depositing the"
CLAIM 26, COLUMN 17, LINE 51,	delete "conformal second layer, and"
CLAIM 26, COLUMN 17, LINE 53,	delete "layer"
CLAIM 26, COLUMN 17, LINE 55,	change "layer;" to --material;--
CLAIM 26, COLUMN 17, LINE 56,	delete "substantially simultaneously subjecting an entire upper"
CLAIM 26, COLUMN 17, LINE 57,	change "surface contour" to --removing a portion-- and change "layer to a" to --material by--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 26,	COLUMN 17, LINE 58,	delete "process and planarizing"
CLAIM 26,	COLUMN 17, LINE 59,	change "layer" to --material-- and delete "therefrom"
CLAIM 26,	COLUMN 17, LINES 61-62,	change "pad oxide layer; and" to --pad oxide;--
CLAIM 26,	COLUMN 17, LINE 63,	change "fusing" to --heat treating the pad oxide, liner, spacers and conformal second material to fuse-- and change "oxide layer," to --oxide,--
CLAIM 26,	COLUMN 17, LINE 64,	change "second layer;" to --second material; and--, insert a paragraph break, and then insert --removing the silicon nitride, first polysilicon material and portions of the pad oxide underlying the silicon nitride such that the conformal second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the pad oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and continue to the upper surface contour of the conformal second material, the sidewalls lie substantially orthogonal to the upper surface contour of the conformal second material;--
CLAIM 29,	COLUMN 18, LINES 9-10,	delete "exposing the pad layer upon a portion of a surface of the semiconductor substrate;"
CLAIM 29,	COLUMN 18, LINE 11,	change "layer upon the" to --upon a--
CLAIM 29,	COLUMN 18, LINE 14,	change "a layer composed of" to --a second--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 29, COLUMN 18,	LINE 15,	after "polysilicon" insert --material-- and delete "layer"
CLAIM 29, COLUMN 18,	LINE 16,	change "spacers," to --spacers;--
CLAIM 29, COLUMN 18,	LINE 17,	change "layer composed of polysilicon" to --second polysilicon material--
CLAIM 30, COLUMN 18,	LINES 21-22,	delete "providing a semiconductor substrate having a top surface with an oxide layer thereon;"
CLAIM 30, COLUMN 18,	LINE 23,	change "a polysilicon layer upon the oxide layer;" to --polysilicon upon an oxide overlying a semiconductor substrate;--
CLAIM 30, COLUMN 18,	LINE 24,	change "first layer" to --first material-- and change "polysilicon layer;" to --polysilicon;--
CLAIM 30, COLUMN 18,	LINE 25,	change "first layer" to --first material--
CLAIM 30, COLUMN 18,	LINE 26,	change "layer to expose the oxide layer at a plurality of areas;" to --to expose a plurality of areas of the oxide;--
CLAIM 30, COLUMN 18,	LINE 28,	change "layer at the plurality of areas," to --at the plurality of areas;--, insert a paragraph break, then insert --implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;-- and then insert another paragraph break
CLAIM 30, COLUMN 18,	LINE 33,	change "oxide layer" to --oxide-- and change "first layer" to --first material--
CLAIM 30, COLUMN 18,	LINE 34,	change "polysilicon layer;" to --polysilicon;--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 30,	COLUMN 18, LINE 37,	change "layer into" to --into--
CLAIM 30,	COLUMN 18, LINE 39,	change "second layer" to --second material--
CLAIM 30,	COLUMN 18, LINE 40,	change "oxide layer" to --oxide--
CLAIM 30,	COLUMN 18, LINE 42,	change "second layer," to --second material,--
CLAIM 30,	COLUMN 18, LINE 44,	change "first layer" to --first material--
CLAIM 30,	COLUMN 18, LINE 45,	change "second layer;" to --second material;--
CLAIM 30,	COLUMN 18, LINE 47,	change "layer and" to --material and--
CLAIM 30,	COLUMN 18, LINE 48,	change "oxide layer," to --oxide,--
CLAIM 30,	COLUMN 18, LINE 51,	change "second layer" to --second material--
CLAIM 30,	COLUMN 18, LINE 53,	change "fusing the oxide layer, spacer and second layer;" to --removing the first material, polysilicon and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and end at the upper surface contour of the second material, the sidewalls are substantially orthogonal to the upper surface contour of the second material;--
CLAIM 30,	COLUMN 18, LINE 55,	change "second layer," to --second material,--
CLAIM 31,	COLUMN 18, LINE 57,	change "as defined in" to --according to--

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Katherine A. Hamer
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 31,	COLUMN 18, LINE 60,	before "doping" insert a paragraph break and then insert --wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide further comprises:--
CLAIM 33,	COLUMN 19, LINES 5-6,	delete "providing a semiconductor substrate having a top surface with an oxide layer thereon;"
CLAIM 33,	COLUMN 19, LINE 7,	change "layer upon the oxide layer;" to --material upon an oxide overlying a semiconductor substrate;--
CLAIM 33,	COLUMN 19, LINE 8,	change "layer to expose the oxide" to --material to expose a plurality of areas of the oxide;--
CLAIM 33,	COLUMN 19, LINE 9,	delete "layer at a plurality of areas;"
CLAIM 33,	COLUMN 19, LINE 11,	delete "layer"
CLAIM 33,	COLUMN 19, LINE 16,	change "oxide layer" to --oxide-- and change "first layer;" to --first material;--
CLAIM 33,	COLUMN 19, LINE 19,	delete "layer"
CLAIM 33,	COLUMN 19, LINE 21,	change "second layer" to --second material--
CLAIM 33,	COLUMN 19, LINE 22,	change "oxide layer" to --oxide--
CLAIM 33,	COLUMN 19, LINE 24,	change "second layer," to --second material,--
CLAIM 33,	COLUMN 19, LINE 26,	change "first layer" to --first material--
CLAIM 33,	COLUMN 19, LINE 27,	change "second layer;" to --second material;--
CLAIM 33,	COLUMN 19, LINE 29,	change "layer" to --material--
CLAIM 33,	COLUMN 19, LINE 30,	change "oxide layer," to --oxide,--
CLAIM 33,	COLUMN 19, LINE 31,	delete "substantially simultaneously subjecting an"

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Katherine A. Hamer
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 33, COLUMN 19,	LINE 32,	change "entire upper surface contour" to --removing portions-- and change "layer to a" to --material by--
CLAIM 33, COLUMN 19,	LINE 33,	change "process; and" to --the entire upper surface contour of the second material;--
CLAIM 33, COLUMN 19,	LINES 34-35,	change "fusing the oxide layer, electrically insulative material, spacer and second layer;" to --implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide; and--, insert a paragraph break and then insert --removing the first material and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material commence at an upper surface of the semiconductor substrate and end at the upper surface contour of the second material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material;--
CLAIM 33, COLUMN 19,	LINE 37,	change "second layer," to --second material,--
CLAIM 34, COLUMN 19,	LINE 41,	change "type;" to --type; and--
CLAIM 34, COLUMN 19,	LINE 42,	delete "and"
CLAIM 36, COLUMN 19,	LINES 57-58,	delete "providing a semiconductor substrate having a top surface with an oxide layer thereon;"

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Katherine A. Hamer
TRASKBRITT
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 36, COLUMN 19, LINE 59,	change "a polysilicon layer upon the oxide layer;" to --polysilicon upon an oxide overlying a semiconductor substrate;--
CLAIM 36, COLUMN 19, LINE 60,	change "first layer" to --first material-- and change "polysilicon layer;" to --polysilicon;--
CLAIM 36, COLUMN 19, LINE 63,	change "oxide layer" to --oxide-- and change "first layer" to --first material--
CLAIM 36, COLUMN 19, LINE 64,	change "polysilicon layer;" to --polysilicon;--
CLAIM 36, COLUMN 19, LINE 65,	delete "from an opening thereto"
CLAIM 36, COLUMN 19, LINE 66,	delete "at top edges at the top surface of the semiconductor"
CLAIM 36, COLUMN 19, LINE 67,	delete "substrate and below the oxide layer"
CLAIM 36, COLUMN 20, LINE 7,	change "oxide layer" to --oxide-- and change "first layer" to --first material--
CLAIM 36, COLUMN 20, LINE 8,	change "polysilicon layer," to --polysilicon,--
CLAIM 36, COLUMN 20, LINE 13,	change "oxide layer" to --oxide-- and change "first layer" to --first material--
CLAIM 36, COLUMN 20, LINE 14,	change "polysilicon layer;" to --polysilicon;--
CLAIM 36, COLUMN 20, LINE 15,	delete "from an opening thereto"
CLAIM 36, COLUMN 20, LINE 16,	delete "at top edges at the top surface of the semiconductor"
CLAIM 36, COLUMN 20, LINE 17,	delete "substrate and below the oxide layer"

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TRASKBRITT
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Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 36,	COLUMN 20, LINE 26,	change "oxide layer" to --oxide-- and change "first layer" to --first material--
CLAIM 36,	COLUMN 20, LINE 27,	change "polysilicon layer," to --polysilicon,--
CLAIM 36,	COLUMN 20, LINE 32,	before "forming" insert --doping the first isolation trench and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide;-- and then insert a paragraph break
CLAIM 36,	COLUMN 20, LINE 35,	change "forming" to --depositing-- and change "layer, composed of" to --material comprising--
CLAIM 36,	COLUMN 20, LINE 36,	before "filling" insert --the conformal second material--
CLAIM 36,	COLUMN 20, LINES 37-38,	change "therebetween and above" to --over remaining portions of-- and delete "layer"
CLAIM 36,	COLUMN 20, LINE 40,	delete "filling is performed by"
CLAIM 36,	COLUMN 20, LINE 41,	delete "depositing the conformal second layer, and"
CLAIM 36,	COLUMN 20, LINE 44,	change "layer" to --material--
CLAIM 36,	COLUMN 20, LINE 45,	change "layer;" to --material;--
CLAIM 36,	COLUMN 20, LINE 46,	change "substantially simultaneously subjecting an entire" to --planarizing portions of the--
CLAIM 36,	COLUMN 20, LINE 47,	change "second layer to a planarizing" to --conformal second material;--
CLAIM 36,	COLUMN 20, LINE 48,	delete "process;"
CLAIM 36,	COLUMN 20, LINE 50,	change "layer" to --material--
CLAIM 36,	COLUMN 20, LINE 52,	change "oxide layer; and" to --oxide;--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 36, COLUMN 20, LINE 53,	change "fusing" to --heat treating the oxide, first spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure;--, then insert a paragraph break and then change "the oxide layer," to --heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide,--
CLAIM 36, COLUMN 20, LINE 54,	change "second layer of the first isolation structure and" to --second material--
CLAIM 36, COLUMN 20, LINE 55,	delete "fusing the oxide layer, first spacer, second spacer and"
CLAIM 36, COLUMN 20, LINE 56,	delete "conformal second layer" and change "structure;" to --structure; and--, insert a paragraph break and then insert --removing the first material, polysilicon and portions of the oxide underlying the first material such that the conformal second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material;--

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 36, COLUMN 20,	LINE 58,	change "layer," to --material,--
CLAIM 37, COLUMN 20,	LINES 62-63,	delete "providing a semiconductor substrate having a top surface with an oxide layer thereon;"
CLAIM 37, COLUMN 20,	LINE 64,	change "layer upon the oxide layer;" to --material upon an oxide overlying a semiconductor substrate;--
CLAIM 37, COLUMN 20,	LINE 67,	change "oxide layer" to --oxide-- and change "first layer;" to --first material;--
CLAIM 37, COLUMN 21,	LINE 1,	delete "from an opening thereto"
CLAIM 37, COLUMN 21,	LINE 2,	delete "at the top surface of the semiconductor substrate and"
CLAIM 37, COLUMN 21,	LINE 3,	delete "below the oxide layer"
CLAIM 37, COLUMN 21,	LINE 9,	change "oxide layer" to --oxide-- and change "first layer," to --first material,--
CLAIM 37, COLUMN 21,	LINE 15,	change "oxide layer" to --oxide-- and change "first layer;" to --first material;--
CLAIM 37, COLUMN 21,	LINE 16,	delete "below the oxide layer"
CLAIM 37, COLUMN 21,	LINE 26,	change "oxide layer" to --oxide-- and change "first layer," to --first material,--
CLAIM 37, COLUMN 22,	LINE 1,	before "forming" insert --doping the first isolation trench and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide;-- and then insert a paragraph break

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Katherine A. Hamer
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,749,860 B2
APPLICATION NO. : 09/392,034
ISSUE DATE : July 6, 2010
INVENTOR(S) : Fernando Gonzalez, David Chapek, and Ranshir P. S. Thakur

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 37,	COLUMN 22, LINE 4,	change "forming" to --depositing-- and change "layer composed of" to --material comprising--
CLAIM 37,	COLUMN 22, LINE 5,	change "material, conformally filling" to --material to fill--
CLAIM 37,	COLUMN 22, LINE 7,	change "therebetween and above the oxide layer" to --over remaining portions of the oxide--
CLAIM 37,	COLUMN 22, LINE 9,	delete "filling is performed"
CLAIM 37,	COLUMN 22, LINE 10,	change "by depositing the conformal second layer, and" to --the--
CLAIM 37,	COLUMN 22, LINE 13,	change "first layer" to --first material--
CLAIM 37,	COLUMN 22, LINE 14,	change "second layer;" to --second material;--
CLAIM 37,	COLUMN 22, LINE 15,	delete "substantially simultaneously subjecting an entire upper"
CLAIM 37,	COLUMN 22, LINE 16,	delete "surface contour of the second layer to a planarizing"
CLAIM 37,	COLUMN 22, LINE 17,	delete "process and" and change "layer" to --material--
CLAIM 37,	COLUMN 22, LINES 19-25,	change "planar upper surface from the conformal the conformal second layer and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches; and" to --planar upper surface;--

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TRASKBRITT
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Salt Lake City, Utah 84102 USA

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

CLAIM 37, COLUMN 22, LINES 26-29, change "fusing the oxide layer, first spacer, second spacer and conformal second layer of the first isolation structure and fusing the oxide layer, first spacer, second spacer and conformal second layer of the second isolation structure." to

--heat treating the oxide, first spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure;--

--heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure; and--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Katherine A. Hamer
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

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PATENT NO : 7,749,860 B2
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims (continued):

--removing the first material and portions of the oxide underlying the first material such that the conformal second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the conformal second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal second material.--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Katherine A. Hamer
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

EXHIBIT A

(NOVEMBER 23, 2009 AMENDMENT)

(Patent No. 7,749,860 B2)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Gonzalez et al.

Serial No.: 09/392,034

Filed: September 8, 1999

For: METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH

Confirmation No.: 9481

Examiner: A. Mai

Group Art Unit: 2814

Attorney Docket No.: 2269-6981.2US
(1996-0723.02/US)

VIA ELECTRONIC FILING

November 23, 2009

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following amendments and remarks are filed in response to the Examiner's remarks in the Office Action mailed August 26, 2009, the three-month shortened statutory period for response to which expires on November 26, 2009.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 25 of this paper.

IN THE CLAIMS:

Claims 1, 5-14, 17-19, 21, 24-26, 31-36, 38, 39, 42 and 43 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming a first dielectric ~~layer~~ material upon an oxide ~~layer~~ over a semiconductor substrate;

selectively removing the first dielectric ~~layer~~ material to expose a plurality of areas of the oxide ~~layer~~;

forming a second dielectric ~~layer~~ material over the first dielectric ~~layer~~ material and in contact with the plurality of exposed areas of the oxide ~~layer~~;

selectively removing the second dielectric ~~layer~~ material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the first dielectric ~~layer~~ material;

removing a portion of material from the plurality of areas of the oxide ~~layer~~ at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench of the plurality of isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

depositing a conformal ~~layer~~ material in each isolation trench, the conformal ~~layer~~ material extending over remaining portions of the oxide ~~layer~~ in contact with a corresponding pair of the spacers, wherein the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer~~ material so as to define an upper surface contour of the conformal ~~layer~~ material;

removing portions of the conformal ~~layer~~ material overlying the remaining portions of the oxide

~~layer~~ by planarizing the conformal ~~layer~~ material at least to the first dielectric ~~layer~~ material and each spacer such that an upper surface for each isolation trench is co-planar to the other upper surfaces,

the conformal ~~layer~~ material comprising a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches; and

removing the first dielectric ~~layer~~ material and portions of the oxide ~~layer~~ underlying the first dielectric ~~layer~~ material such that the conformal ~~layer~~ material fills each said isolation trench, ~~and~~ extends horizontally away from each said isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal material start on an upper surface of the semiconductor substrate and are substantially orthogonal to the upper surface contour of the conformal material.

2. (Canceled).

3. (Previously Presented) The method according to Claim 1, wherein forming a liner upon a sidewall of each isolation trench comprises thermally growing oxide on the semiconductor substrate.

4. (Previously Presented) The method according to Claim 1, wherein forming the liner upon the sidewall of the isolation trench comprises depositing a composition of matter.

5. (Currently amended) The method of claim 1, wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~ comprises forming a doped region below the termination of each of said plurality of the isolation trenches within the semiconductor substrate.

6. (Currently amended) The method according to claim 1, wherein removing portions of the conformal ~~layer~~ material overlying the remaining portions of the oxide ~~layer~~ comprises removing portions of the conformal ~~layer~~ material overlying the remaining portions of the oxide ~~layer~~ by chemical mechanical planarization.

7. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming a first dielectric ~~layer~~material upon an oxide ~~layer~~ over a semiconductor substrate;

selectively removing the first dielectric ~~layer~~ material to expose a plurality of areas of ~~an~~the oxide ~~layer~~;

forming a second dielectric ~~layer~~material over the first dielectric ~~layer~~material and in contact with the plurality of exposed areas of the oxide ~~layer~~;

selectively removing the second dielectric ~~layer~~material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the first dielectric ~~layer~~ material;

removing a portion material from the plurality of areas of the oxide ~~layer~~ at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into the semiconductor substrate;

rounding the top edge of each of the isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

depositing a conformal ~~layer~~material filling each isolation trench, the conformal ~~layer~~ material extending over remaining portions of the oxide ~~layer~~ in contact with a corresponding pair of the spacers, wherein the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer~~ material so as to define an upper surface contour of the conformal ~~layer~~ material;

removing portions of the conformal ~~layer~~ material that overlie the remaining portions of the oxide ~~layer~~ by planarizing the conformal ~~layer~~ material to form an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

removing the first dielectric ~~layer~~ material and portions of the oxide ~~layer~~ underlying the first dielectric ~~layer~~ material such that the conformal ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal material begin on an upper surface of the semiconductor substrate and are oriented substantially orthogonal to the upper surface contour of the conformal material;

wherein:

the conformal ~~layer~~ material comprises ~~a material that~~ is electrically insulative and extends continuously between and within the plurality of isolation trenches;

the conformal ~~layer~~ material and the spacers form the upper surface for each isolation trench, each upper surface being formed from the conformal ~~layer~~ material and the spacer and being situated above the oxide ~~layer~~; and

the first dielectric ~~layer~~ material is in contact with at least a pair of the spacers and the oxide ~~layer~~.

8. (Currently amended) The method according to Claim 7, further comprising:

forming a gate oxide ~~layer~~ upon the semiconductor substrate.

9. (Currently amended The method according to claim 7, wherein removing portions of the conformal ~~layer~~ material comprises etching the material using an etch recipe that etches the conformal ~~layer~~ material faster than the first dielectric ~~layer~~ material by a ratio in a range from about 1:1 to about 2:1.

10. (Currently amended) The method according to Claim 9, wherein etching the material using an etch recipe that etches the conformal ~~layer~~ material faster than the first dielectric ~~layer~~ material by a ratio in a range from about 1:1 to about 2:1 comprises etching the

conformal ~~layer~~ material the ratio is in a range from about 1.3:1 to about 1.7:1.

11. (Currently amended) The method according to claim 7, wherein removing portions of the conformal ~~layer~~ material overlying the remaining portions of the oxide ~~layer~~ comprises:

chemical mechanical planarization, wherein the conformal ~~layer~~ material, the spacers, and the first dielectric ~~layer~~ material form a planar first upper surface; and

etching to form a second upper surface situated above the oxide ~~layer~~.

12. (Currently amended) The method according to Claim ~~11~~7, wherein ~~etching to form a second upper surface~~ removing portions of the conformal material that overlie the remaining portions of the oxide further comprises etching using an etch recipe that etches the conformal ~~layer~~ material faster than the first dielectric ~~layer~~ material by a ratio in a range of from about 1:1 to about 2:1.

13. (Currently amended) The method according to Claim 12, wherein etching using an etch recipe that etches the conformal ~~layer~~ material faster than the first dielectric ~~layer~~ material by a ratio in a range from about 1:1 to about 2:1 comprises etching using an etch recipe that etches the conformal ~~layer~~ material faster than the first dielectric ~~layer~~ material by a ratio in a range of from about 1.3:1 to about 1.7:1.

14. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide ~~layer~~ upon a semiconductor substrate;

forming a silicon nitride ~~layer~~ upon the oxide ~~layer~~;

selectively removing the silicon nitride ~~layer~~ to expose a plurality of areas of the oxide ~~layer~~;

forming a first silicon dioxide ~~layer~~ material over the silicon nitride ~~layer~~ and in contact with the plurality of exposed areas of the oxide ~~layer~~;

selectively removing the first silicon dioxide ~~layer~~ material to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the silicon nitride ~~layer~~;

removing a portion material from the plurality of areas at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches into the semiconductor substrate;

forming a corresponding electrically active region below the termination of each isolation trench within the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

depositing a conformal second silicon dioxide ~~layer~~material filling each isolation trench, the conformal second silicon dioxide ~~layer~~ material within each isolation trench and extending over remaining portions of the oxide ~~layer~~ in contact with the corresponding pair of the spacers, the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and the silicon nitride ~~layer~~ so as to define an upper surface contour of the conformal second silicon dioxide ~~layer~~ material;

removing portions of the conformal second silicon dioxide ~~layer~~ material by planarizing the conformal second silicon dioxide ~~layer~~ material and the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches; and

removing the silicon nitride ~~layer~~ and portions of the oxide ~~layer~~ underlying the silicon nitride ~~layer~~ such that the conformal second silicon dioxide ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the second silicon dioxide material start on an upper surface of the semiconductor substrate and lie substantially orthogonal to the upper surface contour of the second silicon dioxide material.

15. (Previously Presented) The method according to Claim 14, wherein forming a liner upon a sidewall of each isolation trench comprises forming a thermally grown oxide upon a sidewall of the semiconductor substrate.

16. (Previously Presented) The method according to Claim 14, wherein forming a liner upon a sidewall of each isolation trench comprises forming a liner composed of silicon nitride.

17. (Currently amended) The method according to Claim 15, further comprising:
forming a gate oxide ~~layer~~ upon the semiconductor substrate.

18. (Currently amended) A method of forming a microelectronic structure, the method comprising:
forming an oxide ~~layer~~ upon a semiconductor substrate;
forming ~~a~~ polysilicon ~~layer~~ upon the oxide ~~layer~~;
forming a first dielectric ~~layer~~ material upon the polysilicon ~~layer~~;
selectively removing the first dielectric ~~layer~~ material and the polysilicon ~~layer~~ to expose a plurality of areas of the oxide ~~layer~~;
forming a second dielectric ~~layer~~ material conformally over the polysilicon ~~layer~~, the first dielectric ~~layer~~ material and in contact with the plurality of exposed areas of the oxide ~~layer~~;
selectively removing the second dielectric ~~layer~~ material to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the first dielectric ~~layer~~ material;
removing a portion of material from the plurality of areas of the oxide ~~layer~~ at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;
rounding the top edges of each of the isolation trenches;
implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a

plane of the oxide ~~layer~~;

depositing a conformal third ~~layer~~ material filling each isolation trench, the conformal third ~~layer~~ material extending over remaining portions of the oxide ~~layer~~ in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer~~ material so as to define an upper surface contour of the conformal third ~~layer~~ material;

removing portions of the conformal third ~~layer~~ material by planarizing the conformal third ~~layer~~ material to form an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

removing the first dielectric ~~layer~~ material, polysilicon ~~layer~~ and portions of the oxide ~~layer~~ underlying the first dielectric ~~layer~~ material such that the conformal third ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third ~~layer~~ material, and the plurality of isolation trenches.

19. (Currently amended) The method according to Claim 18, wherein removing portions of the conformal third ~~layer~~ material comprises removing portions of the conformal third ~~layer~~ material by chemical mechanical planarization.

20. (Previously Presented) The method according to Claim 18, wherein implanting comprises forming a doped region below the termination of each isolation trench within the semiconductor substrate.

21. (Currently amended) The method according to Claim 18, wherein rounding the top edges of each of the isolation trenches comprises forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide ~~layer~~ to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third ~~layer~~ material is ~~composed of an~~ electrically insulative ~~material~~.

22. (Previously Presented) The method according to Claim 21, wherein forming a liner upon a sidewall of each isolation trench comprises forming a thermally grown oxide upon a sidewall the semiconductor substrate.

23. (Canceled).

24. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide ~~layer~~ upon a semiconductor substrate;

forming ~~a~~ polysilicon ~~layer~~ upon the oxide ~~layer~~;

forming a first dielectric ~~layer~~ material upon the polysilicon ~~layer~~;

selectively removing the first dielectric ~~layer~~ material and the polysilicon ~~layer~~ to expose a plurality of areas of the oxide ~~layer~~;

forming a second dielectric ~~layer~~ material over the polysilicon ~~layer~~, the first dielectric ~~layer~~ material and in contact with the plurality of exposed areas of the oxide ~~layer~~;

selectively removing the second dielectric ~~layer~~ material to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the first dielectric ~~layer~~ material;

removing a portion of material from the plurality of exposed areas of the oxide ~~layer~~ at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a

plane of the oxide ~~layer~~;

depositing a conformal third ~~layer~~ material filling each isolation trench, the conformal third ~~layer~~ material extending over remaining portions of the oxide ~~layer~~ in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer~~ material so as to define an upper surface contour of the conformal third ~~layer~~ material;

removing portions of the conformal third ~~layer~~material by planarizing the conformal third ~~layer~~ material to form an upper surface for each isolation trench of the plurality of isolation trenches that is co-planar to the other upper surfaces;

removing the first dielectric ~~layer~~ material, polysilicon ~~layer~~ and portions of the oxide ~~layer~~ underlying the first dielectric ~~layer~~ material such that the conformal third ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material,

wherein the conformal third ~~layer~~material is ~~an~~ electrically insulative ~~material that~~ and extends continuously between and within the plurality of isolation trenches;

wherein the upper surface for each isolation trench of the plurality of isolation trenches is formed from the conformal third ~~layer~~material, the spacers, and the first dielectric ~~layer~~material; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third ~~layer~~material, and the plurality of isolation trenches.

25. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide ~~layer~~ upon a semiconductor substrate;

forming a first polysilicon ~~layer~~ material upon the oxide ~~layer~~;

forming a first dielectric ~~layer~~ material upon the polysilicon ~~layer~~;

selectively removing the first dielectric ~~layer~~ material and the first polysilicon ~~layer~~ material to expose a plurality of areas of the oxide ~~layer~~;

forming a second dielectric ~~layer~~ material over the first dielectric ~~layer~~ material and in contact with the plurality of exposed areas of the oxide ~~layer~~;

selectively removing the second dielectric ~~layer~~ material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the first dielectric ~~layer~~ material;

removing a portion of material from the plurality of exposed areas of the oxide ~~layer~~ at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

rounding the top edges of each of the isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

depositing a conformal third ~~layer~~material filling each isolation trench, the conformal third ~~layer~~ material extending over remaining portions of the oxide ~~layer~~ in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer~~ material so as to define an upper surface contour of the conformal third ~~layer~~ material;

removing portions of the conformal third ~~layer~~material overlying the remaining portions of the oxide ~~layer~~ by planarizing the conformal third ~~layer~~material to form an upper surface for each isolation trench that is co-planar to the other upper surfaces;

exposing the oxide ~~layer~~ upon a portion of a surface of the semiconductor substrate;

forming a gate oxide ~~layer~~ upon the portion of the surface of the semiconductor substrate;

forming between the plurality of isolation trenches, and confined in the space therebetween, a ~~layer composed of~~ second polysilicon material upon the oxide ~~layer~~ in contact with a pair of the spacers;

selectively removing the third material~~layer~~, the spacers, and the ~~layer composed of~~ second polysilicon material to form a portion of at least one of the upper surfaces; and

removing the first dielectric ~~layer~~ material, first polysilicon material ~~layer~~ and portions of the

oxide ~~layer~~ underlying the first dielectric ~~layer~~ material such that the conformal third ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate and extend to the upper surface contour of the conformal third material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

26. (Currently amended) A method of forming a microelectronic structure, the method comprising:

~~forming an oxide layer upon a semiconductor substrate;~~

forming ~~a~~ polysilicon ~~layer~~ upon ~~the~~an oxide overlying a semiconductor substrate~~layer~~;

forming a first dielectric ~~layer~~ material upon the polysilicon ~~layer~~;

selectively removing the first dielectric ~~layer~~ material and the polysilicon ~~layer~~ to expose a plurality of areas of the oxide ~~layer~~;

forming a second dielectric ~~layer~~ material over the polysilicon ~~layer~~ and the first dielectric ~~layer~~ material and in contact with the plurality of exposed areas of the oxide ~~layer~~;

selectively removing the second dielectric ~~layer~~material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the first dielectric ~~layer~~ material;

removing material from the plurality of exposed areas of the oxide ~~layer~~ at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

rounding the top edges of each isolation trench of the plurality of isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

depositing a conformal third ~~layer~~material filling each isolation trench, the conformal third ~~layer~~ material extending over remaining portions of the oxide ~~layer~~ in contact with a

corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer~~material so as to define an upper surface contour of the conformal third ~~layer~~material;

removing portions of the conformal third ~~layer~~material overlying the remaining portions of the oxide ~~layer~~ by planarizing the conformal third ~~layer~~material to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces using an etch recipe that etches the conformal third ~~layer~~material and the spacers faster than the first dielectric ~~layer~~ material by a ratio of from about 1:1 to about 2:1;

heat treating the oxide ~~layer~~, spacers and conformal third ~~layer~~ material to fuse the oxide ~~layer~~, spacers and conformal third ~~layer~~ material;

removing the first dielectric ~~layer~~ material, polysilicon ~~layer~~ and portions of the oxide ~~layer~~ underlying the first dielectric ~~layer~~ material such that the conformal third ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third ~~layer~~ material, and the plurality of isolation trenches.

27. (Previously Presented) The method according to claim 26, wherein the ratio is in a range from about 1.3:1 to about 1.7:1.

28-30 (Canceled).

31. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming a pad oxide ~~layer~~ upon a semiconductor substrate;

forming a first polysilicon ~~layer~~ material upon the oxide ~~layer~~;

forming ~~a~~ silicon nitride ~~layer~~ upon the first polysilicon ~~layer~~ material;

selectively removing the silicon nitride ~~layer~~ and the first polysilicon ~~layer~~ material to expose a plurality of areas of the oxide ~~layer~~;

forming a first silicon dioxide ~~layer~~ material over the silicon nitride ~~layer~~ and in contact with the exposed oxide ~~layer~~ at the plurality of exposed areas of the oxide ~~layer~~;

selectively removing the first silicon dioxide ~~layer~~ material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the silicon nitride ~~layer~~ and the polysilicon ~~layer~~;

removing a portion of material from the plurality of exposed areas at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

forming a corresponding doped region below the termination of each isolation trench within the semiconductor substrate by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

forming a liner upon a sidewall of each isolation trench, each liner extending from an interface thereof with the oxide ~~layer~~ to the termination of the isolation trench within the semiconductor substrate;

rounding the top edges of the isolation trenches;

depositing a conformal second ~~layer~~material filling each isolation trench, the conformal second ~~layer~~material extending over remaining portions of the oxide ~~layer~~ in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the silicon nitride ~~layer~~ so as to define an upper surface contour of the conformal second ~~layer~~material;

removing a portion of the conformal second ~~layer~~ material by planarizing the conformal second ~~layer~~ material and each of the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and is situated above the oxide ~~layer~~; and

heat treating the oxide ~~layer~~, liner, spacers and conformal second ~~layer~~ material to fuse the oxide ~~layer~~, liner, spacers and conformal second ~~layer~~ material;

removing the silicon nitride ~~layer~~, first polysilicon ~~layer~~ material and portions of the oxide ~~layer~~ underlying the silicon nitride ~~layer~~ such that the conformal second ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and continue to the upper surface contour of the conformal second material, the sidewalls lie substantially orthogonal to the upper surface contour of the conformal second material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

32. (Currently amended) The method according to Claim 31, wherein each liner is a thermally grown oxide of the semiconductor substrate, and wherein the conformal second ~~layer~~ material is ~~composed of an~~ electrically insulative ~~material~~.

33. (Currently amended) The method according to Claim 31, wherein each liner is composed of silicon nitride, and wherein the conformal second ~~layer~~ material is ~~composed of an~~ electrically insulative ~~material~~.

34. (Currently amended) The method according to Claim 31, further comprising:

forming a gate oxide ~~layer~~ upon a portion of the surface of the semiconductor substrate;

forming between the plurality of isolation trenches, and confined in the space therebetween, a ~~layer composed of~~ second polysilicon material upon the gate oxide ~~layer~~ in contact with a pair of the spacers, and

selectively removing ~~the layer composed of~~ the second polysilicon material to form a portion of at least one of the upper surfaces.

35. (Currently amended) A method for forming a microelectronic structure, the method comprising:

forming ~~a~~ polysilicon ~~layer~~ upon an oxide ~~layer~~ overlying a semiconductor substrate;

forming a first ~~layer~~ material upon the polysilicon ~~layer~~;

selectively removing the first ~~layer~~ material and the polysilicon ~~layer~~ to expose a plurality of areas of the oxide ~~layer~~;

forming a plurality of isolation trenches through the exposed oxide ~~layer~~ at the plurality of areas;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches, each isolation trench:

having a spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material and the polysilicon ~~layer~~;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide ~~layer~~ into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second ~~layer~~ material filling the isolation trench and extending above the oxide ~~layer~~ in contact with the spacer, wherein filling is performed by depositing the second ~~layer~~ material, and depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first ~~layer~~ material so as to define an upper surface contour of the second ~~layer~~material; and

having a planar upper surface formed from the second ~~layer~~material and the spacer and being situated above the oxide ~~layer~~, wherein the planar upper surface is formed by substantially simultaneously subjecting the entire upper surface contour of the second ~~layer~~ material to a planarizing process; and

removing the first ~~layer~~ material, polysilicon ~~layer~~ and portions of the oxide ~~layer~~ underlying the first ~~layer~~ material such that the second ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and end at the upper surface contour of the second material, the sidewalls are substantially orthogonal to the upper surface contour of the second material;

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second ~~layer~~ material, and the plurality of isolation trenches.

36. (Currently amended) The method according to claim 35,

doping the semiconductor substrate with a dopant having a first conductivity type;

and wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~ further comprises:

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one isolation trench of the plurality of isolation trenches.

37. (Previously Presented) The method according to claim 36, wherein the doped trench bottom has a width, each isolation trench has a width, and the width of each doped trench bottom is greater than the width of the respective isolation trench.

38. (Currently amended) A method for forming a microelectronic structure, the method comprising:

forming a first ~~layer~~ material upon an oxide ~~layer~~ overlying a semiconductor substrate;

selectively removing the first ~~layer~~ material to expose a plurality of areas of the oxide ~~layer~~;

forming a plurality of isolation trenches through the oxide ~~layer~~ at the plurality of areas, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches without filling the plurality of isolation trenches, each isolation trench:

having a spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide ~~layer~~ into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second ~~layer~~ material filling the isolation trench and extending above the oxide ~~layer~~ in contact with the spacer, wherein the filling is performed by depositing the second ~~layer~~ material, and the depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first ~~layer~~ material so as to define an upper surface contour of the second ~~layer~~ material; and

having a planar upper surface formed from the second ~~layer~~ material and the spacer and being situated above the oxide ~~layer~~, wherein the planar upper surface is formed by removing portions of the second ~~layer~~ material by planarizing the entire upper surface contour of the second ~~layer~~ material;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~; and

removing the first ~~layer~~ material and portions of the oxide ~~layer~~ underlying the first ~~layer~~ material such that the second ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the second material commence at an upper surface of the semiconductor substrate and end at the upper surface contour of the second material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material;

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second ~~layer~~ material, and the plurality of isolation trenches.

39. (Currently amended) The method according to claim 38, further comprising:
doping the semiconductor substrate with a dopant having a first conductivity type;
and wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~ further comprises;
doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of the isolation trenches.

40. (Previously Presented) The method of claim 39, wherein:
the doped trench bottom has a width;
each isolation trench has a width; and
the width of each doped trench bottom is greater than the width of the respective isolation trench.

41. (Canceled).

42. (Currently amended) A method for forming a microelectronic structure, the method comprising:
forming ~~a~~ polysilicon ~~layer~~ upon an oxide ~~layer~~ overlying a semiconductor substrate;
forming a first ~~layer~~ material upon the polysilicon ~~layer~~;
forming a first isolation structure including:
a first spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material and the polysilicon ~~layer~~;
a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and
a second spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material and the polysilicon ~~layer~~, the second spacer being situated on a

side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material and the polysilicon ~~layer~~;

a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is curved; and

a second spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material and the polysilicon ~~layer~~, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

rounding the top edges of the isolation trenches;

doping the first isolation trench and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

depositing a conformal second ~~layer~~ material comprising an electrically insulative material, the conformal second ~~layer~~ material filling the first and second isolation trenches and extending continuously over remaining portions of the oxide ~~layer~~ in contact with the first and second spacers of the respective first and second isolation structures, depositing is carried out to the extent of filling each of the isolation trenches and extending over the spacers and over the first ~~layer~~ material so as to define an upper surface contour of the conformal second ~~layer~~ material;

planarizing portions of the upper surface contour of the conformal second ~~layer~~ material;

forming a planar upper surface from the conformal second ~~layer~~ material and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide ~~layer~~;

heat treating the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer~~ material of the first isolation structure to fuse the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer~~ material of the first isolation structure;

heat treating the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer~~ material of the second isolation structure to fuse the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer~~ material of the second isolation structure, and

removing the first ~~layer~~ material, polysilicon ~~layer~~ and portions of the oxide ~~layer~~ underlying the first ~~layer~~ material such that the conformal second ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material;

wherein the microelectronic structure is defined at least in part by the active area, the second ~~layer~~ material, and the first and second isolation trenches.

43. (Currently amended) A method for forming a microelectronic structure, the method comprising:

forming a first ~~layer~~ material upon an oxide ~~layer~~ overlying a semiconductor substrate;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material;

a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material;

a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the first ~~layer~~ material, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

doping the first isolation trench and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

depositing a conformal second ~~layer~~ material comprising an electrically insulative material to fill the first and second isolation trenches and extending continuously over remaining portions of the oxide ~~layer~~ in contact with the first and second spacers of the respective first and second isolation structures, wherein the depositing is carried out to the extent of filling each of the isolation trenches and extending over the spacers and over the first ~~layer~~ material so as to define an upper surface contour of the conformal second ~~layer~~ material;

planarizing the conformal second ~~layer~~ material and the first and second spacers of the respective first and second isolation structures to form a planar upper surface;

heat treating the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer~~ material of the first isolation structure to fuse the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer~~ material of the first isolation structure;

heat treating the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer~~ material of

the second isolation structure to fuse the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer~~ material of the second isolation structure; and

removing the first ~~layer~~ material and portions of the oxide ~~layer~~ underlying the first ~~layer~~ material such that the conformal second ~~layer~~ material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the conformal second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal second material.

REMARKS

The Office Action mailed August 26, 2009, has been received and reviewed. Claims 1, 3 through 22, 24 through 27, 31 through 40, 42 and 43 are currently pending in the application. Claims 1, 3 through 22, 24 through 27, 31 through 40, 42 and 43 stand rejected. Applicants have amended claims 1, 5-14, 17-19, 21, 24-26, 31-36, 38, 39, 42 and 43. Each of claims 1, 5-14, 17-19, 21, 24-26, 31-36, 38, 39, 42 and 43 have been amended to replace the word "layer" with "material" and/or to remove the word "layer." Support for additional amendments to claims 1, 7, 14, 18, 24-26, 31, 35, 38, 42 and 43 may be found throughout the as-filed specification including, for example, page 16, lines 3-7. Support for additional amendments to claim 12 may be found throughout the as-filed specification for example, page 14, lines 14-22 and FIG. 7A/7B. Reconsideration is respectfully requested.

Drawing Objection

The drawings are objected to under 37 CFR §1.83(a). The Examiner asserts that the drawings do not show the elements of claim 12 of "etching to form a second upper surface comprises etching using an etch recipe that etch the conformal layer faster than the first dielectric layer." Applicants respectfully traverse this rejection, as hereinafter set forth. Claim 12 has been amended to recite "The method according to Claim 7, wherein removing portions of the conformal material that overlie the remaining portions of the oxide further comprises etching using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range of from about 1:1 to about 2:1." Support for the amendment may be found throughout the as-filed specification for example, page 14, lines 14-22 and FIG. 7A/7B. Reconsideration and withdrawal of the rejection is requested.

35 U.S.C. § 112 Claim Rejections

Claims 12 and 13 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had

possession of the claimed invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 12 and 13 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully traverse this rejection, as hereinafter set forth. Claim 12 has been amended to recite "The method according to Claim 7, wherein removing portions of the conformal material that overlie the remaining portions of the oxide further comprises etching using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range of from about 1:1 to about 2:1." Support for the amendment may be found throughout the as-filed specification for example, page 14, lines 14-22. Reconsideration and withdrawal of the rejection is requested.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor in View of U.S. Patent No. 5,387,540 to Poon et al.

Claims 1, 3 through 9, 11 through 22, 24 through 26, 31 through 40, 42 and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072) in view of Poon et al. (U.S. Patent No. 5,387,540). Applicants respectfully traverse this rejection, as hereinafter set forth.

To establish a *prima facie* case of obviousness the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Additionally, the Examiner must determine whether there is "an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1740-1741, 167 L.Ed.2d 705, 75 USLW 4289, 82 U.S.P.Q.2d 1385 (2007). Further, rejections on obviousness grounds "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id* at 1741, quoting *In re Kahn*, 441, F.3d 977, 988 (Fed. Cir. 2006). To establish a *prima facie* case of obviousness there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097

(Fed. Cir. 1986). Furthermore, the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge, or the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

Omid-Zohoor discloses a method of forming trenches with suppressed parasitic edge transistors. Trenches 360 are formed in a substrate 120 having a pad oxide layer 340 and silicon nitride layer 344 thereon. (Omid-Zohoor, FIG. 3I). Spacers 356 may flank the trenches 360. A thick oxide layer 364 is deposited to cover the wafer and fill the trenches 360. A reverse mask 368 is placed over defined trench regions. The mask is followed by an etch which creates oxide ridges. (Omid-Zohoor, col. 4, lines 47-55, FIG. 3L). The upper surface of the oxide layer 372 is polished to expose the silicon nitride layer 344. (*Id.*, FIG. 3M). The silicon nitride layer 344 is removed, but the pad oxide layer 340 remains. (*Id.* at col. 5, lines 2-4). Portions of the overfilled oxide 376 and pad oxide 344 are removed together resulting in slight oxide humps above the trenches. (*Id.*, FIG. 3N).

Poon is cited for teaching the formation of a liner along the sidewall of a trench. (Office Action mailed February 20, 2009, page 5).

The proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide" or "removing the first dielectric material and portions of the oxide underlying the first dielectric material such that the conformal material fills each said isolation trench, ~~and~~ extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal material start on an upper surface of the semiconductor substrate and are substantially orthogonal to the upper surface contour of the conformal material" as recited in independent claim 1. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide."

Poon, col. 2, lines 59-64.

The proposed combination of references does not teach or suggest "removing the first dielectric material and portions of the oxide underlying the first dielectric material such that the conformal material fills each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal material start on an upper surface of the semiconductor substrate and are substantially orthogonal to the upper surface contour of the conformal material" as recited in independent claim 1. Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 and portions of the overfilled oxide 376 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal material start on an upper surface of the semiconductor substrate and are substantially orthogonal to the upper surface contour of the conformal material" as recited in claim 1 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed. Specifically, Omid-Zohoor states:

> As shown in FIG. 3N, when the silicon nitride is removed by etch, the pad oxide serves as an etch stop and the overfilled oxide 376 remains.
> Next, in FIG. 3O, the pad oxide in the active region is etched such that it is substantially removed from the surface of the substrate 120. However, in the area of the trenches 360, oxide humps 376 remain with a top level above the surface of the substrate 120. Portions of the oxide humps 376 cover the edges and corner of the trenches 360.

(Omid-Zohoor, col. 5, lines 2-10). Omid-Zohoor fails to teach or suggest that the upper surface contour of the overfilled oxide 376 is substantially orthogonal to the sidewalls of the overfilled oxide 376 as recited in claim 1 of the presently claimed invention. Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As the proposed combination of references fails to teach or suggest each and every limitation of independent claim 1, Omid-Zohoor in view of Poon cannot render

claim 1 obvious. Accordingly, claim 1 is allowable.

Claims 3-6 are each allowable as depending from allowable claim 1.

With respect to independent claim 7, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," or "removing the first dielectric material and portions of the oxide underlying the first dielectric material such that the conformal material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal material begin on an upper surface of the semiconductor substrate and are oriented substantially orthogonal to the upper surface contour of the conformal material" as recited in claim 7 of the presently claimed invention. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 and portions of the overfilled oxide 376 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal material begin on an upper surface of the semiconductor substrate and are oriented substantially orthogonal to the upper surface contour of the conformal material" as recited in claim 7 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As the proposed combination of references fails to teach or suggest each and every limitation of claim 7, Omid-Zohoor in view of

Poon cannot render claim 7 obvious. Accordingly, independent claim 14, and dependent claims 8, 9, 11 and 12 therefrom, are allowable.

With respect to independent claim 14, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," or "removing the silicon nitride and portions of the oxide underlying the silicon nitride such that the conformal second silicon dioxide material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second silicon dioxide material start on an upper surface of the semiconductor substrate and lie substantially orthogonal to the upper surface contour of the second silicon dioxide material" as recited in claim 14 of the presently claimed invention. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 and portions of the overfilled oxide 376 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the second silicon dioxide material start on an upper surface of the semiconductor substrate and lie substantially orthogonal to the upper surface contour of the second silicon dioxide material" as recited in claim 14 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As the proposed combination of references fails to teach or suggest each and every limitation of claim 14, Omid-Zohoor in view

of Poon cannot render claim 14 obvious. Accordingly, independent claim 14, and dependent claims 15-17 therefrom, are allowable.

With respect to independent claim 18, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the third conformal material and are substantially orthogonal to the upper surface contour of the conformal third material" or "wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches" as recited in independent claim 18. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the third conformal material and are substantially orthogonal to the upper surface contour of the conformal third material" as recited in claim 18 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As Omid-Zohoor in view of Poon fails to teach or suggest this limitation, the proposed combination of art likewise fails to teach or suggest that "the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches" as recited in claim 18.

As the proposed combination of references fails to teach or suggest each and every limitation of independent claim 18, Omid-Zohoor in view of Poon cannot render claim 18 obvious. Accordingly, claim 18 is allowable.

Claims 19-22 are each allowable, at least, as depending from allowable claim 18.

With respect to independent claim 24, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material" or "wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches" as recited in independent claim 24. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from

each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material" as recited in claim 24 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As Omid-Zohoor in view of Poon fails to teach or suggest this limitation, the proposed combination of art likewise fails to teach or suggest that "the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches" as recited in claim 24.

As the proposed combination of references fails to teach or suggest each and every limitation of independent claim 24, Omid-Zohoor in view of Poon cannot render claim 24 obvious. Accordingly, claim 24 is allowable.

With respect to independent claim 25, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," or "removing the first dielectric material, first polysilicon material and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate and extend to the upper surface contour of the conformal third material, the sidewalls lie substantially orthogonal to the upper surface contour of the conformal third material" as recited in claim 25 of the presently claimed invention. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at pp. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate and extend to the upper surface contour of the conformal third material, the sidewalls lie substantially orthogonal to the upper surface contour of the conformal third material" as recited in claim 25 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As the proposed combination of references fails to teach or suggest each and every limitation of claim 25, Omid-Zohoor in view of Poon cannot render claim 25 obvious. Accordingly, claim 25 is allowable.

With respect to independent claim 26, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "heat treating the oxide, spacers and conformal third material to fuse the oxide, spacers and conformal third material" "removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material" or "wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches as recited in claim 26. The Examiner acknowledges that Omid-

Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material" as recited in claim 26 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As Omid-Zohoor in view of Poon fails to teach or suggest this limitation, the proposed combination of art likewise fails to teach or suggest that "the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches" as recited in claim 26.

Further, the Examiner does not identify any portion of Omid-Zohoor or Poon that teaches or suggests "heat treating the oxide, spacers and conformal third material to fuse the oxide, spacers and conformal third material" as recited in claim 26.

As the proposed combination of references fails to teach or suggest each and every limitation of claim 26, Omid-Zohoor in view of Poon cannot render claim 26 obvious. Accordingly, claim 26 is allowable.

With respect to independent claim 31, the proposed combination of Omid-Zohoor and

Poon fails to teach or suggest "forming a corresponding doped region below the termination of each isolation trench with a semiconductor substrate by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "heat treating the oxide, liner, spacers and conformal second material to fuse the oxide, liner spacers and conformal second material" or "removing the silicon nitride, first polysilicon material and portions of the oxide underlying the silicon nitride such that the conformal second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and continue to the upper surface contour of the conformal second material and the sidewalls lie substantially orthogonal to the upper surface contour of the conformal second material" as recited in claim 31. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and continue to the upper surface contour of the conformal second material and the sidewalls lie substantially orthogonal to the upper surface contour of the conformal second material" as recited in claim 31 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). Further, the Examiner does not identify

any portion of Omid-Zohoor or Poon that teaches or suggests "heat treating the oxide, liner, spacers and conformal second material to fuse the oxide, liner spacers and conformal second material" as recited in claim 31.

As the proposed combination of references fails to teach or suggest each and every limitation of claim 31, Omid-Zohoor in view of Poon cannot render claim 31 obvious. Accordingly, claim 31 is allowable.

Claims 32-34 are each allowable, at least, as depending from allowable claim 31.

With respect to independent claim 35, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and end at the upper surface contour of the second material, the sidewalls are substantially orthogonal to the upper surface contour of the second material" or "wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches" as recited in independent claims 18, 24 and 35. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and end at the upper surface

contour of the second material, the sidewalls are substantially orthogonal to the upper surface contour of the second material" as recited in claim 35 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As Omid-Zohoor in view of Poon fails to teach or suggest this limitation, the proposed combination of art likewise fails to teach or suggest that "the microelectronic structure is defined at least in part by the plurality of spacers, the second material, and the plurality of isolation trenches" as recited in claim 35.

As the proposed combination of references fails to teach or suggest each and every limitation of independent claim 35, Omid-Zohoor in view of Poon cannot render claim 35 obvious. Accordingly, claim 35 is allowable. Claims 36 and 37 are each allowable as depending from allowable claim 35.

Claim 36 is further allowable as the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "doping the semiconductor substrate with dopant having a first conductivity type; and wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide further comprises; doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of the isolation trenches" as recited in claim 36. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p 7). Poon lacks any teaching or suggestion that ions are dopants of two different conductivities may be used. Poon, col. 2, lines 59-64. As the proposed combination of references fails to teach or suggest each and every limitation of claim 36, Omid-Zohoor in view of Poon cannot render claim 36 obvious. Accordingly, claim 36 is allowable.

Claim 37 is further allowable as the proposed combination of Omid-Zohoor and Poon fails to teach or suggest that "the doped trench bottom has a width; each isolation trench has a width and the width of each doped trench bottom is greater than the width of the respective

isolation trench" as recited in claim 37. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon lacks any teaching or suggestion of the respective width of the trench compared to the trench bottom. As the proposed combination of references fails to teach or suggest each and every limitation of claim 37, Omid-Zohoor in view of Poon cannot render claim 37 obvious. Accordingly, claim 37 is allowable.

With respect to independent claim 38, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," or "removing the first material and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material commence at an upper surface of the semiconductor substrate and end at the upper surface contour of the second material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material, wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second material and the plurality of isolation trenches" as recited in claim 38. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the second material commence at an upper surface of the semiconductor substrate and end at the upper surface contour of the second material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material" as recited in claim 38 because in Omid-Zohoor,

the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As Omid-Zohoor in view of Poon, fails to teach or suggest this limitation, the proposed combination of art likewise fails to teach or suggest that "the microelectronic structure is defined at least in part by the plurality of spacers, the second material, and the plurality of isolation trenches" as recited in claim 38.

As the proposed combination of references fails to teach or suggest each and every limitation of claim 38, Omid-Zohoor in view of Poon cannot render claim 38 obvious. Accordingly, claim 38 is allowable.

In addition to the reasons submitted with respect to independent claim 38, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "doping the semiconductor substrate with dopant having a first conductivity type; and wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide further comprises; doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of the isolation trenches" as recited in claim 39. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p 7). Poon lacks any teaching or suggestion that ions are dopants of two different conductivities may be used. Poon, col. 2, lines 59-64.

As the proposed combination of references fails to teach or suggest each and every limitation of claim 39, Omid-Zohoor in view of Poon cannot render claim 39 obvious. Accordingly, claim 39 is allowable.

In addition to the reasons submitted with respect to claims 38 and 39, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest that "the doped trench bottom has a width; each isolation trench has a width and the width of each doped trench bottom is

greater than the width of the respective isolation trench" as recited in claim 40. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon lacks any teaching or suggestion of the respective width of the trench compared to the trench bottom.

As the proposed combination of references fails to teach or suggest each and every limitation of claim 40, Omid-Zohoor in view of Poon cannot render claim 40 obvious. Accordingly, claim 40 is allowable.

With respect to independent claim 42, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "doping the first isolation trench and second isolation trench by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "heat treating the oxide, first spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure," "heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure" or "removing the first material and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material wherein the microelectronic structure is defined at least in part by the active area, the second material and the first and second isolation trenches" as recited in claim 42. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in

slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material" as recited in claim 42 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). As Omid-Zohoor in view of Poon fails to teach or suggest this limitation, the proposed combination of art likewise fails to teach or suggest that "the microelectronic structure is defined at least in part by the active area, the second material, and the first and second isolation trenches" as recited in claim 42.

Further, the Examiner does not identify any portion of Omid-Zohoor or Poon that teaches or suggests "heat treating the oxide, first spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure," or "heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure" as recited in claim 42.

As the proposed combination of references fails to teach or suggest each and every limitation of claim 42, Omid-Zohoor in view of Poon cannot render claim 42 obvious. Accordingly, claim 42 is allowable.

With respect to independent claim 43, the proposed combination of Omid-Zohoor and Poon fails to teach or suggest "doping the first isolation trench and second isolation trench by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "heat treating the oxide, first spacer, second spacer and conformal second

material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure," "heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure" or "removing the first material and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material" as recited in claim 43. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material" as recited in claim 43 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon fails to cure the deficiencies of Omid-Zohoor. Instead, Poon teaches that trench plug 34 has substantially vertical sidewalls. (Poon, FIG. 6). Further, the Examiner does not identify any portion of Omid-Zohoor or Poon that teaches or suggests "heat treating the oxide, first

spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure," or "heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure" as recited in claim 43.

As the proposed combination of references fails to teach or suggest each and every limitation of claim 43, Omid-Zohoor in view of Poon cannot render claim 43 obvious. Accordingly, claim 43 is allowable.

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor in View of U.S. Patent No. 5,387,540 to Poon et al., U.S. Patent No. 5,858,858 to Park et al. and U.S. Patent No. 6,069,083 to Miyashita et al.

Claims 26 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072) in view of Poon et al. (U.S. Patent No. 5,387,540), Park et al. (U.S. Patent 5,858,858) and Miyashita et al. (U.S. Patent No. 6,069,083). Applicants respectfully traverse this rejection, as hereinafter set forth.

The discussion of Omid-Zohoor and Poon above is incorporated herein. Park is cited for teaching the formation of a trench and for heat treatment to densify the conformal layer. (Office Action sent August 26, 2009, page 28). Miyashita *et al.* teaches methods of CMP and is cited for teaching a planarization process which etches the conformal layer and spacers faster than the first dielectric layer by a ratio of from about 1:1 to about 2:1. (Office Action sent August 26, 2009, page 29).

The proposed combination of Omid-Zohoor and Poon, Park and Miyashita fails to teach or suggest "implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material, the

sidewalls are substantially orthogonal to the upper surface contour of the conformal third material" or "wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches as recited in claim 26. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 27). Park also fails to teach or suggest ion implantation. Poon and Miyashita fail to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." *See* Poon, col. 2, lines 59-64; Miyashita, col. 1, lines 24-34.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material, the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material" as recited in claim 26 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon, Park and Miyashita fail to cure the deficiencies of Omid-Zohoor. Instead, Park and Poon teaches that trench plug (24A)(34) has substantially vertical sidewalls and does not extends horizontally away from the isolation trench. (Poon, FIG. 6; Park FIGs. 7 and 8). Similarly, Miyashita fails to teach or suggest this limitation. (Miyashita, FIGs. 5M, 6D). As Omid-Zohoor in view of Poon, Park and Miyashita fails to teach or suggest this limitation, the proposed combination of art likewise fails to teach or suggest that "the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches."

As the proposed combination of references fails to teach or suggest each and every limitation of claim 26, Omid-Zohoor in view of Poon, Park and Miyashita cannot render claim 26 obvious. Accordingly, independent claim 26 and dependent claim 27 therefrom are allowable.

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor in View of U.S. Patent No. 5,387,540 to Poon et al. and U.S. Patent No. 5,858,858 to Park et al.

Claims 31 through 34, 42 and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072) in view of Poon et al. (U.S. Patent No. 5,387,540) and Park et al. (U.S. Patent No. 5,858,858). Applicants respectfully traverse this rejection, as hereinafter set forth.

The discussion of Omid-Zohoor, Poon and Park above is incorporated herein. The proposed combination of Omid-Zohoor in view of Poon and Park fails to teach or suggest "forming a corresponding doped region below the termination of each isolation trench with a semiconductor substrate by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," or "removing the silicon nitride, first polysilicon material and portions of the oxide underlying the silicon nitride such that the conformal second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and continue to the upper surface contour of the conformal second material and the sidewalls lie substantially orthogonal to the upper surface contour of the conformal second material" as recited in claim 31. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 31). Park also fails to teach or suggest ion implantation. Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in

slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and continue to the upper surface contour of the conformal second material and the sidewalls lie substantially orthogonal to the upper surface contour of the conformal second material" as recited in claim 31 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon and Park fail to cure the deficiencies of Omid-Zohoor. Instead, Poon and Park teach that trench plug (24a) 34 has substantially vertical sidewalls and does not extends horizontally away from the isolation trench. (Poon, FIG. 6; Park FIGs. 7 and 8).

As the proposed combination of references fails to teach or suggest each and every limitation of claim 31, Omid-Zohoor in view of Poon and Park cannot render claim 31 obvious. Accordingly, independent claim 31 and dependent claims 32-34 therefrom are allowable.

With respect to independent claim 42, the proposed combination of Omid-Zohoor, Poon and Park fails to teach or suggest "doping the first isolation trench and second isolation trench by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "heat treating the oxide, first spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure," "heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure" or "removing the first material and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the

second material wherein the microelectronic structure is defined at least in part by the active area, the second material and the first and second isolation trenches" as recited in claim 42. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 27). Park also fails to teach or suggest ion implantation. Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material" as recited in claim 42 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon and Park fail to cure the deficiencies of Omid-Zohoor. Instead, Poon and Park teach that trench plug (24a) 34 has substantially vertical sidewalls and does not extends horizontally away from the isolation trench. (Poon, FIG. 6; Park FIGs. 7 and 8). As Omid-Zohoor in view of Poon fails to teach or suggest this limitation, the proposed combination of art likewise fails to teach or suggest that "the microelectronic structure is defined at least in part by the active area, the second material, and the first and second isolation trenches" as recited in claim 42.

As the proposed combination of references fails to teach or suggest each and every limitation of claim 42, Omid-Zohoor in view of Poon and Park cannot render claim 42 obvious. Accordingly, claim 42 is allowable.

With respect to independent claim 43, the proposed combination of Omid-Zohoor and

Poon fails to teach or suggest "doping the first isolation trench and second isolation trench by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide," "heat treating the oxide, first spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure," "heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure" or "removing the first material and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material" as recited in claim 43. The Examiner acknowledges that Omid-Zohoor fails to teach or suggest implantation of ions. (Office Action sent August 26, 2009 at p. 7). Park also fails to teach or suggest ion implantation. Poon fails to teach or suggest that ions are implanted "in a direction substantially orthogonal to a plane of the oxide." Poon, col. 2, lines 59-64.

Omid-Zohoor teaches removing portions of the overfilled oxide 376 and silicon nitride layer 344 while the pad oxide layer 340 under the silicon nitride layer 344 remains. (Omid-Zohoor, col. 4, lines 60-62; FIG. 3N). The next step removes the pad oxide 340 resulting in slight oxide humps above the trenches. (*Id.*, col. 5, lines 5-10; FIG. 3O). Thus, the resulting overfilled oxide 376 does not "fill each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material" as recited in claim 43 because in Omid-Zohoor, the pad oxide 340 and horizontal portions of the overfilled oxide 376 are removed and the overfilled oxide 376 lacks any surface which is substantially orthogonal to the sidewalls of the overfilled oxide 376.

Poon and Park fail to cure the deficiencies of Omid-Zohoor. Instead, Poon and Park teach that trench plug (24a) 34 has substantially vertical sidewalls and does not extends horizontally away from the isolation trench. (Poon, FIG. 6; Park FIGs. 7 and 8). As the proposed combination of references fails to teach or suggest each and every limitation of claim 43, Omid-Zohoor in view of Poon and Park cannot render claim 43 obvious. Accordingly, claim 43 is allowable.

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor and U.S. Patent No. 5,387,540 to Poon et al. and Further in View of U.S. Patent No. 6,069,083 to Miyashita et al.

Claims 9 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072) and Poon et al. (U.S. Patent No. 5,387,540) as applied to claims 7 and 11 above and further in view of Miyashita et al. (U.S. Patent No. 6,069,083). Applicants respectfully traverse this rejection, as hereinafter set forth.

The Court of Appeals for the Federal Circuit has stated that Adependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.@ In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP ' 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 9 and 10 obvious, cannot serve as a basis for rejection.

Obviousness Rejection Based on U.S. Patent No. 6,097,072 to Omid-Zohoor and U.S. Patent No. 5,387,540 to Poon et al. and Further in View of U.S. Patent No. 4,963,502 to Teng et al.

Claims 36, 37, 39 and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072) and Poon et al. (U.S. Patent No. 5,387,540) as applied to claims 35 and 38 above and further in view of Teng et al. (U.S. Patent No. 4,963,502). Applicants respectfully traverse this rejection, as hereinafter set forth.

The discussion of Omid-Zohoor and Poon above is incorporated herein. Teng et al. is cited for teaching providing a p+ semiconductor substrate and implanting dopants in trenches to produce N-wells. (Teng, col. 6, lines 55-59; Office Action sent August 26, 2009, page 39). Teng fails to cure the deficiencies of Omid-Zohoor and Poon.

The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 36, 37, 39 and 40 obvious, cannot serve as a basis for rejection.

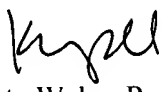
ENTRY OF AMENDMENTS

The amendments to claims 1, 5-14, 17-19, 21, 24-26, 31-36, 38, 39, 42 and 43 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1, 3-22, 24-27, 31-40, 42 and 42, are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, the Examiner is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



Krista Weber Powell
Registration No. 47,867
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: November 23, 2009
KAH/kso/tlp
Document in ProLaw

EXHIBIT B

(RULE 312 AMENDMENT DATED APRIL 23, 2010)

(Patent No. 7,749,860 B2)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Gonzalez *et al.*

Serial No.: 09/392,034

Filed: September 8, 1999

For: METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH

Confirmation No.: 9481

Examiner: A. Mai

Group Art Unit: 2814

Attorney Docket No.: 2269-6981.2US
(1996-0723.02/US)

Notice of Allowance Dated:

January 27, 2010

VIA ELECTRONIC FILING
APRIL 23, 2010

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the specification begin on page 3 of this paper;

Amendments to the Abstract appear on page 13 of this paper;

Amendments to the claims are set forth in the listing of the claims that begins on page 14 of this paper;

Corrections to the drawings are summarized on page 34 of this paper, with replacement sheets and four (4) annotated sheets showing the corrections enclosed herewith; and

Remarks start at page 35 of this paper.

IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a continuation of U.S. Patent Application Serial No. 08/985,588, filed ~~on~~ December 5, 1997, now U.S. Patent No. 5,953,621, issued September 14, 1999, which is a divisional ~~patent application~~ of U.S. Patent Application Serial No. 08/823,609, filed ~~on~~ March 25, 1997, now U.S. Patent No. 6,097,076, issued August 1, 2000, both of which are incorporated herein by reference.

Please amend paragraph **[0008]** as follows:

[0008] An active area may be formed within semiconductor substrate 12 immediately beneath pad oxide 14, and adjacent isolation material 48. A problem that is inherent in such non-planarity of fill material within an isolation trench is that corners 62 may leave the active area of semiconductor substrate 12 exposed. As such, isolation material 48 will not prevent layers formed thereon from contacting the active area of semiconductor substrate 12 at corners 62. Contact of this sort is detrimental in that it causes charge and current leakage. Isolation material 48 is also unable to prevent unwanted thermal oxide encroachment through corners 62 into the active area of semiconductor substrate 12.

Please amend paragraph **[0009]** as follows:

[0009] What is needed is a method of forming an isolation trench, where subsequent etching of fill material within the isolation trench of such method prevents overlying layers from having contact with an adjacent active area, and prevents unwanted thermal oxide encroachment into the active area. What is also needed is a method of forming an isolation trench wherein etching or planarizing such as by ~~chemical mechanical~~ chemical-mechanical planarization (CMP) of isolation trench materials is accomplished without forming a recess at the intersection of the fill material in the isolation trench and the material of the active area within the semiconductor substrate.

Please amend paragraph **[0013]** as follows:

[0013] A third dielectric layer is formed substantially conformably over the spacer and the first dielectric layer so as to substantially fill the isolation trench. Topographical reduction of the third dielectric layer follows, preferably so as to planarize the third dielectric ~~layer for example by chemical mechanical~~ layer, for example, by chemical-mechanical planarizing (CMP), by dry etchback, or by a combination thereof.

Please amend paragraph **[0014]** as follows:

[0014] The topographical reduction of the third dielectric layer may also be carried out as a single etchback step that sequentially removes superficial portions of the third dielectric layer that extend out of the isolation trench. The single etchback also removes portions of the remaining spacer, and removes substantially all of the remaining portions of the first dielectric layer. Preferably, the single etchback will use an etch recipe that is more selective to the third dielectric layer and the spacer than to the remaining portions of the first dielectric layer. The single etchback uses an etch recipe having a selectivity that will preferably leave a raised portion of the third dielectric layer extending above the isolation trench while removing substantially all remaining portions of the first dielectric layer. The resulting structure can be described as having the shape of a nail as viewed in a direction that is substantially orthogonal to the ~~cross-section~~ cross-section of a word line in association therewith.

Please amend paragraph **[0025]** as follows:

[0025] FIGS. 5A and 5B illustrate further processing of the ~~structure~~ structures depicted, respectively, in FIGS. 4A and 4B, in which the insulation film has been etched to form a spacer, a simultaneous or serial etch has formed an isolation trench, thermal oxidation or deposition within the isolation trench has formed an insulation liner therein, and wherein an optional ion implantation has formed a doped region at the bottom of the isolation trench.

Please amend paragraph **[0026]** as follows:

[0026] FIGS. 6A and 6B illustrate further processing of the ~~structure~~ structures depicted, respectively, in FIGS. 5A and 5B, in which an isolation film has been deposited over the spacer, the isolation trench within the isolation trench liner, and the nitride island.

Please amend paragraph **[0027]** as follows:

[0027] FIGS. 7A and 7B illustrate further processing of the ~~structure~~ structures depicted, respectively, in FIGS. 6A and 6B, wherein a planarization process has formed a first upper surface made up of the nitride island, the spacer, and the isolation film, all being substantially co-planar on the first upper surface.

Please amend paragraph **[0028]** as follows:

[0028] FIG. 8A illustrates further processing of the ~~structure~~ structures depicted in FIGS. 7A or 9A, wherein the semiconductor substrate has been implanted with ions, and wherein the isolation film, optionally the pad oxide layer, the insulation liner, and the spacer have fused to form a unitary isolation structure.

Please amend paragraph **[0029]** as follows:

[0029] FIG. 8B illustrates optional further processing of the ~~structure~~ structures depicted in FIG. 6B, wherein an etching process using an etch recipe that is slightly selective to oxide over nitride, has etched back the isolation film, the nitride island, and the spacer to expose the polysilicon island, and has formed a filled isolation trench which, when viewed in a direction that is substantially orthogonal to the ~~cross-section~~ cross-section of the depicted word line, has the shape of a nail.

Please amend paragraph **[0030]** as follows:

[0030] FIG. 9A illustrates optional further processing of the ~~structure~~ structures depicted in FIG. 6A or in FIG. 7A, wherein an etch-selective recipe that is slightly selective to

oxide over nitride has formed a filled isolation trench which, when viewed in ~~cross-section,~~ cross-section has the shape of a nail.

Please amend paragraph **[0031]** as follows:

[0031] FIG. 9B illustrates further processing of the ~~structure~~ structures depicted in either FIGS. 7B or 8B wherein the semiconductor substrate has been implanted with ions, and wherein the isolation film, optionally the pad oxide layer, the insulation liner, and the spacer have been fused to form a filled isolation trench.

Please amend paragraph **[0036]** as follows:

[0036] FIG. 4A illustrates further processing of the structure depicted in FIG. 3A, wherein an insulation film 26 has been deposited upon insulator island 22 and exposed portions of pad oxide 14. Insulation film 26 can be an oxide such as silicon dioxide, and can be formed for example by decomposition of tetraethyl ~~ortho silicate~~ orthosilicate (TEOS). Insulation film 26 may also be formed by a plasma enhanced chemical vapor deposition (PECVD) process so as to deposit a nitride layer such as ~~Si.sub.3N.sub.4~~ Si_3N_4 or equivalent. When insulation film 26 is a nitride layer, insulator island 22 would be selected to be composed of a substantially different material, such as an oxide. Formation of substantially different materials between insulator island 22 and insulation film 26 facilitate selective etchback or selective mechanical planarization such as chemical-mechanical polishing (CMP) in the inventive method of forming an isolation trench.

Please amend paragraph **[0037]** as follows:

[0037] Following deposition of insulation film 26, a spacer etch and an isolation trench etch are carried out. The spacer etch and the isolation trench etch can be carried out with a single etch recipe that is selective to insulation film 26. Alternatively, the spacer etch and the isolation trench etch can be carried out with two etch recipes. As such, the first etch etches insulation film 26 in a spacer etch that forms a spacer 28 seen in FIG. 5A. The second etch, or isolation trench etch, has an etch recipe that is selective to spacer 28 and insulator island 22, and

anisotropically etches an isolation trench 32 having a ~~side wall~~ sidewall 50 in semiconductor substrate 12.

Please amend paragraph **[0041]** as follows:

[0041] Insulation liner 30 may be substantially composed of a nitride such as ~~Si.sub.3N.sub.4,~~ Si_3N_4, or an equivalent, and can be selectively formed upon sidewall 50 of isolation trench 32. When semiconductor substrate 12 immediately adjacent to isolation trench 32 is a doped monocrystalline silicon that forms, for example, an active area for a transistor source/drain region, oxidation is avoided therein by insulation liner 30. Insulation liner is preferably substantially composed of ~~Si.sub.3N.sub.4~~ Si_3N_4 or a non-stoichiometric variant ~~which~~ that seals sidewall 50 so as to prevent encroachment of oxide into semiconductor substrate 12.

Please amend paragraph **[0042]** as follows:

[0042] Following formation of insulation liner 30, ion implantation is optionally carried out to form a doped trench bottom 34 at the bottom of isolation trench 32. For example, if semiconductor wafer 10 comprises an N-doped silicon substrate, implantation of P-doping materials at the bottom of isolation trench 32 will form a P-doped trench bottom 34. Ion implantation may be carried out in a field implantation mode. If a complementary metal oxide semiconductor (CMOS) is being fabricated, however, masking of ~~complimentary~~ complementary regions of semiconductor substrate 12 is required in order to achieve the differential doping thereof. For an N-doped silicon substrate, a high breakdown voltage may be achieved by P-doping. A low breakdown voltage may be achieved by N-doping, and an intermediate breakdown voltage may be achieved by no doping. Because the present invention relates to formation of isolation trenches, P-doping in an N-well region, or N-doping in a P-well region are preferred.

Please amend paragraph **[0047]** as follows:

[0047] It is preferable, at some point in fabrication of the isolation trench, to densify the fill material of the isolation trench. Densification is desirable because it helps to prevent separation of materials in contact with the fill material. As seen in FIG. 6A, densification will prevent isolation film 36 from separating at interfaces with spacer 28, pad oxide ~~layer~~ 14, and insulation liner 30. It is preferable to perform densification of isolation film 36 immediately following its deposition. Depending upon the specific application, however, densification may be carried out at other stages of the process. For example, densification of isolation film 36 by rapid thermal processing (RTP) may make either etchback or CMP more difficult. As such, it is preferable to densify later in the fabrication process, such as after planarizing or etchback processing.

Please amend paragraph **[0048]** as follows:

[0048] FIG. 7A illustrates a subsequent step of formation of the isolation trench wherein insulator island 22, spacer 28, and isolation film 36 are planarized to a common co-planar first upper surface 38. First upper surface 38 will preferably be formed by a CMP or etchback process. Preferably, planarization will ~~remove to~~ remove isolation film 36 slightly faster than insulator island 22, such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, wherein isolation film 36 is removed faster as compared to insulator ~~island.~~ island 22. A more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred selectivity is about 1.5:1. Planarization also requires the etch recipe to remove spacer 28 slightly faster than insulator island 22. ~~Preferably~~ Preferably, spacer 28 and ~~insulator~~ isolation film 36 are made from the same material such that the etch will be substantially uniform as to the selectivity thereof with respect to spacer 28 and isolation film 36 over insulator island 22.

Please amend paragraph **[0049]** as follows:

[0049] First upper surface 38 is illustrated as being substantially planar in FIG. 7A. It will be appreciated by one of ordinary skill in the art that first upper surface 38 will form a

non-planar profile or topography depending upon the selectivity of the etch recipe or of the chemical used in a planarization technique such as CMP. For example, where reduced island 52 is formed from a nitride material and isolation film 36 is formed from an oxide material, first upper surface 38 would undulate as viewed in ~~cross section~~ cross-section with more prominent structures being the result of an etch or planarization technique more selective thereto.

Please amend paragraph **[0052]** as follows:

[0052] Phantom lines 60 in FIG. 8A illustrate remnants of pad oxide ~~layer~~ 14, insulation liner 30, and spacer 28 as they are optionally thermally fused with isolation film 36 to form isolation structure 48. Isolation structure 48, illustrated in FIG. 8A, comprises a trench portion and a flange portion which together, when viewed in ~~cross section,~~ cross-section, form the shape of a nail.

Please amend paragraph **[0053]** as follows:

[0053] The trench portion of isolation structure 48 is substantially composed of portions of isolation film 36 and insulation liner 30. The trench portion intersects the flange portion at a second upper surface 40 of semiconductor substrate 12 as seen in FIG. 8A. The trench portion also has two sidewalls 50. FIG. 8A shows that the trench portion is substantially parallel to a third upper surface 42 and sidewalls 50. The flange portion is integral with the trench portion and is substantially composed of portions of pad oxide ~~layer~~ 14, spacer 28, and isolation film 36. The flange portion has a lowest region at second upper surface 40 where the flange portion intersects the trench portion. The flange portion extends above second upper surface 40 to third upper surface 42 seen in FIG. 8A. Upper surfaces 40, 42 are substantially orthogonal to two flange sidewalls 64 and sidewall 50. The flange portion is substantially orthogonal in orientation to the trench portion. The flange portion may also include a gate oxide layer 44 after gate oxide layer 44 is grown.

Please amend paragraph **[0057]** as follows:

[0057] Gate oxide layer 44 is formed upon second upper surface 40 after pad oxide 14 has been removed to form portions of third upper surface 42. The entirety of third upper surface 42 includes head 54 of isolation structure 48 as it extends above gate oxide layer 44 ~~and gate oxide layer 44~~.

Please amend paragraph **[0058]** as follows:

[0058] In a variation of the first embodiment of the present invention, the structure illustrated in FIG. 6A is planarized by use of a single etchback process. The single etchback uses an etch recipe that has a different selectivity for insulator island 22 than for isolation film 36. In this alternative embodiment, spacer 28, ~~dielectric~~ isolation film 36, and pad oxide 14 are composed of substantially the same material. Insulator island 22 has a composition different from that of isolation film 36. For example, isolation film 36 and spacer 28 are composed of ~~SiO.sub.2,~~ SiO_2, and insulator island 22 is composed of silicon nitride.

Please amend paragraph **[0061]** as follows:

[0061] A starting structure for an example of a second embodiment of the present invention is illustrated in FIG. 2B. In FIG. 2B, pad oxide ~~layer~~ 14 is grown upon semiconductor substrate 12 and a polysilicon layer 18 is deposited upon pad oxide ~~layer~~ 14. This embodiment of the present invention parallels the processing steps of the first embodiment with the additional processing that takes into account the use of polysilicon layer 18.

Please amend paragraph **[0062]** as follows:

[0062] FIG. 3B illustrates etching through nitride layer 16 and polysilicon layer 18 to stop on pad oxide ~~layer~~ 14. The etch creates both an insulator island 22 and a polysilicon island 24 formed, respectively, from nitride layer 16 and polysilicon layer 18.

Please amend paragraph **[0063]** as follows:

[0063] FIG. 4B illustrates further processing of the structure depicted in FIG. 3B, wherein insulation film 26 has been deposited upon insulator island 22, laterally exposed portions of polysilicon island 24, and exposed portions of pad oxide ~~layer~~ 14. Following deposition of insulation film 26, a spacer etch and an isolation trench etch are carried out similarly to the spacer etch and isolation trench etch carried out upon semiconductor structure 10 illustrated in FIG. 5A.

Please amend paragraph **[0064]** as follows:

[0064] FIG. 5B illustrates the results of both the spacer etch and the isolation trench etch and optional implantation of isolation trench 32 to form ~~doped well~~ trench bottom 34 analogous to doped trench bottom 34 illustrated in FIG. 5A. Formation of insulation liner 30 within isolation trench 32 preferentially precedes implantation to form ~~doped~~ P-doped trench bottom 34. Following optional implantation of doping ions, full or partial removal of spacer 28 may optionally be performed as set forth above with respect to the first embodiment of the invention.

Please amend paragraph **[0068]** as follows:

[0068] To form the structure seen in FIG. 9B, semiconductor structures 10 of FIGS. 7B or 8B are subjected to implantation of semiconductor substrate 12 with ions. Semiconductor structure 10 is then subjected to a heat treatment so as to fuse together isolation film 36, optional pad oxide ~~layer~~ 14, insulation liner ~~60,~~ 30, and spacer 28 into an integral filled isolation trench.

Please amend paragraph **[0069]** as follows:

[0069] Subsequent to the process illustrated in FIGS. 6A-8A and 6B-9B a final thermal treatment, or subsequent thermal treatments, can be performed. Heat treatment may cause isolation structure 48 to be wider proximal to third upper surface 42 than proximal to doped trench bottom 34. When so shaped, an unoxidized portion of the active area of semiconductor substrate 12 that forms sidewall 50 would have a trapezoidal shape when viewed in ~~cross-section,~~

cross-section, where the widest portion is second upper surface 40 and the narrowest portion is at doped trench bottom 34. Where a trapezoidal shape of the trench portion causes unwanted encroachment into the active area of semiconductor substrate 12, the optional formation of insulation liner 30 from a nitride material or equivalent is used to act as an oxidation barrier for sidewall 50. Semiconductor structure 10 is illustrated in FIG. 9B as being implanted by doping ions, as depicted with ~~downwardly directed~~ downwardly directed arrows. Following a preferred implantation, thermal processing may be carried out in order to achieve dopant diffusion near upper surface 42b of implanted ions residing within semiconductor substrate 12. Due to head 54 extending onto semiconductor substrate 12, a doping concentration gradient can be seen between the active area 53a and the active area 53b. The starting and stopping point of the doping concentration gradient in relation to flange sidewalls 64 will depend upon the duration and temperature of a thermal treatment.

Please amend paragraph **[0070]** as follows:

[0070] The present invention may be carried out wherein spacer 28 and isolation film 36 are substantially composed of the same oxide material, and insulator island 22 is substantially ~~composes~~ composed of a nitride composition. Other compositions may be chosen wherein etch selectivity or CMP selectivity slightly favors insulator island 22 over both spacer 28 and isolation film 36. The specific selection of materials will depend upon the application during fabrication of the desired isolation trench.

IN THE ABSTRACT:

Please amend the Abstract originally appearing on page 45 of the application as follows:

ABSTRACT OF THE DISCLOSURE

The present invention relates to a method for forming an isolation trench structure in a semiconductor substrate without causing deleterious topographical depressions in the upper surface thereof which cause current and charge leakage to an adjacent active area. The inventive method forms a pad oxide upon a semiconductor substrate, and then forms a nitride layer on the pad oxide. The nitride layer is patterned with a mask and etched to expose a portion of the pad oxide layer and to protect an active area in the semiconductor substrate that remains covered with the nitride layer. A second dielectric layer is formed substantially conformably over the pad oxide layer and the remaining portions of the first dielectric layer. A spacer etch is then carried out to form a spacer from the second dielectric layer. The spacer is in contact with the remaining portion of the first dielectric layer. An isolation trench etch follows the spacer etch. An optional thermal oxidation of the surfaces in the isolation trench may be performed, which may optionally be followed by doping of the bottom of the isolation trench to further isolate neighboring active regions on either side of the isolation trench. A conformal layer is formed substantially conformably over the spacer, over the remaining portions of the first dielectric layer, and substantially filling the isolation trench. Planarization of the conformal layer follows, either by CMP or by etchback or by a combination thereof. An isolation trench filled with a structure results. The resulting structure has a flange and shaft, the ~~cross-section~~ cross-section of which has a nail shape in ~~cross-section.~~ cross-section.

IN THE CLAIMS:

Claims 2, 23, 28 through 30, and 41 were previously cancelled. Claims 1, 5, 6, 7, 11, 14, 18, 19, 24, 25, 26, 31, 34, 35, 36, 38, 42, and 43 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon the oxide layer;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer over the oxide layer and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer over and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer into the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

forming a liner upon a sidewall of each isolation trench;

filling each isolation trench with a conformal layer, the conformal layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein the filling is performed by depositing the conformal layer, and the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal ~~layer; and~~ layer;

substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal layer at least to the first dielectric

layer and each spacer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

fusing the oxide layer, liner, spacers and conformal layer;

wherein the conformal layer comprises a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches.

2. (Cancelled)

3. (Previously presented) The method according to Claim 1, wherein the liner is a thermally grown oxide of the semiconductor substrate.

4. (Previously presented) The method according to Claim 1, wherein forming the liner upon the sidewall of the isolation trench comprises deposition of a composition of matter.

5. (Currently amended) The method according to Claim 1, further comprising forming a doped region below the termination of ~~each the~~ each isolation trench within the semiconductor substrate.

6. (Currently amended) The method according to Claim 1, wherein the upper surface for ~~each the~~ each isolation trench is formed by ~~chemical-mechanical~~ chemical-mechanical planarization.

7. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming a first dielectric layer upon an oxide layer over a semiconductor substrate;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer over the oxide layer and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer into the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has an edge;

rounding ~~the~~ a top edge of each of the plurality of isolation trenches;

filling each isolation trench with a conformal layer, the conformal layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal layer and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal layer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

fusing the oxide layer, spacers and conformal layer;

wherein:

the conformal layer comprises a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches;

the conformal layer and the spacers form the upper surface for each isolation trench, each upper surface being formed from the conformal layer and the ~~spacer~~ spacers and being situated above the oxide layer; and

the first dielectric layer is in contact with at least a pair of the spacers and the oxide layer.

8. (Previously presented) The method according to Claim 7, further comprising:

removing the oxide layer upon a portion of a surface of the semiconductor substrate; and

forming a gate oxide layer upon the portion of the surface of the semiconductor substrate.

9. (Previously presented) The method according to Claim 7, wherein planarizing the conformal layer comprises using an etch recipe that etches the conformal layer faster than the first dielectric layer by a ratio in a range from about 1:1 to about 2:1.

10. (Previously presented) The method according to Claim 9, wherein the ratio is in a range from about 1.3:1 to about 1.7:1.

11. (Currently amended) The method according to Claim 7, wherein the upper surface for ~~each the~~ each isolation trench is formed by:

~~chemical-mechanical~~ chemical-mechanical planarization, wherein the conformal layer, the spacers, and the first dielectric layer form a planar first upper surface; and

an etch that forms a second upper surface, the second upper surface being situated above ~~the pad~~ the oxide layer.

12. (Previously presented) The method according to Claim 11, wherein the etch uses an etch recipe that etches the conformal layer faster than the first dielectric layer by a ratio in a range from about 1:1 to about 2:1.

13. (Previously presented) The method according to Claim 12, wherein the ratio is in a range from about 1.3:1 to about 1.7:1.

14. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon the oxide layer;

selectively removing the silicon nitride layer to expose the oxide layer at a plurality of areas;

forming a first silicon dioxide layer over the oxide layer and over the silicon nitride layer, wherein forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer to form a plurality of spacers from the first silicon dioxide layer, wherein each spacer is situated upon the oxide layer, is in contact with the silicon nitride layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer into and terminating within the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

forming a corresponding electrically active region below the termination of each isolation trench within the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer to the termination of the isolation trench within the semiconductor substrate;

filling each isolation trench with a conformal second silicon dioxide layer, the conformal second silicon dioxide layer within each isolation trench extending above the oxide layer in contact with the corresponding pair of the spacers, wherein filling is performed by depositing the conformal second silicon dioxide layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and the silicon nitride layer so as to define an upper surface contour of the conformal second silicon dioxide layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the conformal second silicon dioxide layer to a planarizing process so as to remove the conformal second silicon dioxide layer and the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above ~~the pad~~ the oxide layer, wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

fusing the oxide layer, liner, spacers and conformal second silicon dioxide layer.

15. (Previously presented) The method according to Claim 14, wherein the liner is a thermally grown oxide of the semiconductor substrate.

16. (Previously presented) The method according to Claim 14, wherein the liner is composed of silicon nitride.

17. (Previously presented) The method according to Claim 15, further comprising:
removing the oxide layer upon a portion of a surface of the semiconductor substrate; and
forming a gate oxide layer upon the portion of the surface of the semiconductor substrate.

18. (Currently amended) A method of forming a microelectronic structure, the method comprising:
forming an oxide layer upon a semiconductor substrate;
forming a polysilicon layer upon the oxide layer;
forming a first dielectric layer upon the polysilicon layer;
selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;
forming a second dielectric layer conformally over the oxide layer, the polysilicon layer, and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;
selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer is upon the oxide layer, is in contact with both the polysilicon layer and the first dielectric layer, and is adjacent to an area of the plurality of areas;
forming a plurality of isolation trenches extending below the oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;
rounding the top edges of each of the isolation trenches;

filling each isolation trench with a conformal third layer, the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal third layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal third layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the conformal third layer to a planarizing process and planarizing the conformal third layer to form therefrom an upper surface for each ~~said~~ isolation trench that is co-planar to the other ~~said~~ upper surfaces; and

fusing the oxide layer, spacers and conformal third layer;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

19. (Currently amended) The method according to Claim 18, wherein the upper surface for each isolation trench is formed by ~~chemical-mechanical~~ chemical-mechanical planarization.

20. (Previously presented) The method according to Claim 18, further comprising forming a doped region below the termination of each isolation trench within the semiconductor substrate.

21. (Previously presented) A method according to Claim 18, wherein rounding the top edges of each of the isolation trenches comprises forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third layer is composed of an electrically insulative material.

22. (Previously presented) The method according to Claim 21, wherein the liner is a thermally grown oxide of the semiconductor substrate.

23. (Cancelled)

24. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over the oxide layer, the polysilicon layer, and the first dielectric layer, wherein forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer is upon the oxide layer, is in contact with both the polysilicon layer and the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

rounding the top edges of each isolation trench of the plurality of isolation trenches;

filling each isolation trench of the plurality of isolation trenches with a conformal third layer, the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal third layer, and depositing is carried out to the extent of filling each isolation trench and extending

over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal third layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the conformal third layer to a planarizing process and planarizing the conformal third layer to form therefrom an upper surface for each isolation trench of the plurality of isolation trenches that is co-planar to the other upper surfaces; and

fusing the oxide layer, spacers and conformal third ~~layer~~ layer;

wherein the conformal third layer is an electrically insulative material that extends continuously between and within the plurality of isolation trenches;

wherein the upper surface for each isolation trench of the plurality of isolation trenches is formed from the conformal third layer, the spacers, and the first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

25. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over the oxide layer, the polysilicon layer, and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer of the plurality of spacers is upon the oxide layer, is in contact with both the polysilicon layer and the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

rounding the top edges of each of the isolation trenches;

filling each isolation trench with a conformal third layer, the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal third layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal third layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the conformal third layer to a planarizing process and planarizing the conformal third layer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces;

exposing the oxide layer upon a portion of a surface of the semiconductor substrate;

forming a gate oxide layer upon the portion of the surface of the semiconductor substrate;

forming between the plurality of isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with a pair of the spacers;

selectively removing the third layer, the spacers, and the layer composed of polysilicon to form a portion of at least one of the upper surfaces; and

fusing the oxide layer, spacers and conformal third layer;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

26. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over the oxide layer, the polysilicon layer, and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer of the plurality of spacers is upon the oxide layer, is in contact with both the polysilicon layer and the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

rounding the top edges of each isolation trench of the plurality of isolation trenches;

filling each isolation trench with a conformal third layer, the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal third layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal third layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the conformal third layer to a planarizing process comprising an etch recipe that etches the conformal third layer and the spacers faster than the first dielectric by a ratio in a range ~~from of~~ from about 1:1 to about 2:1 and planarizing the conformal third layer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

fusing the oxide layer, spacers and conformal third layer;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

27. (Previously presented) The method according to Claim 26, wherein the ratio is in a range from about 1.3:1 to about 1.7:1.

28.-30. (Cancelled)

31. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the pad oxide layer;

forming a silicon nitride layer upon the polysilicon layer;

selectively removing the silicon nitride layer and the polysilicon layer to expose the pad oxide layer at a plurality of areas;

forming a first silicon dioxide layer over the pad oxide layer and over the silicon nitride layer, wherein the forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed pad oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer to form a plurality of spacers from the first silicon dioxide layer, wherein each spacer of the plurality of spacers is situated upon the pad oxide layer, is in contact with the silicon nitride layer and the polysilicon layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the pad oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

forming a corresponding doped region below the termination of each isolation trench within the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench, each liner extending from an interface thereof with the pad oxide layer to the termination of the isolation trench within the semiconductor substrate;

rounding the top edges of the isolation trenches;

filling each isolation trench with a conformal second layer, the conformal second layer extending above the pad oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal second layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the silicon nitride layer so as to define an upper surface contour of the conformal second layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the conformal second layer to a planarizing process and planarizing the conformal second layer and each of the spacers to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces and is situated above the pad oxide layer; and

fusing the pad oxide layer, liner, spacers and conformal second layer;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

32. (Previously presented) The method according to Claim 31, wherein each liner is a thermally grown oxide of the semiconductor substrate, and wherein the conformal second layer is composed of an electrically insulative material.

33. (Previously presented) The method according to Claim 31, wherein each liner is composed of silicon nitride, and wherein the conformal second layer is composed of an electrically insulative material.

34. (Currently amended) The method according to Claim 31, further comprising:
exposing the pad oxide layer upon a portion of a surface of the semiconductor substrate;
forming a gate oxide layer upon the portion of the surface of the semiconductor substrate;
forming between the plurality of isolation trenches, and confined in ~~the~~ a space therebetween, a layer composed of polysilicon upon the gate oxide layer in contact with a pair of the spacers, and
selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surfaces.

35. (Currently amended) A method for forming a microelectronic structure, the method comprising:
providing a semiconductor substrate having a top surface with an oxide layer thereon;
forming a polysilicon layer upon the oxide layer;
forming a first layer upon the polysilicon layer;
selectively removing the first layer and the polysilicon layer to expose the oxide layer at a plurality of areas;
forming a plurality of isolation trenches through the exposed oxide layer at the plurality of areas, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches, each isolation trench:
having a spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer filling the isolation trench and extending above the oxide layer in contact with the spacer, wherein filling is performed by depositing the second layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first layer so as to define an upper surface contour of the second layer; and

having a planar upper surface formed from the second layer and the spacer and being situated above the oxide layer, wherein the planar upper surface is formed by substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the second layer to a planarizing process; and

fusing the oxide layer, spacer and second layer;

wherein the microelectronic structure is defined at least in part by ~~the~~ a plurality of spacers, the second layer, and the plurality of isolation trenches.

36. (Currently amended) The method as defined in Claim 35, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity ~~type;~~ type; and

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one isolation trench of the plurality of isolation trenches.

37. (Previously presented) The method as defined in Claim 36, wherein the doped trench bottom has a width, each isolation trench has a width, and the width of each doped trench bottom is greater than the width of the respective isolation trench.

38. (Currently amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon the oxide layer;

selectively removing the first layer to expose the oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the oxide layer at the plurality of areas, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches without filling the plurality of isolation trenches, each isolation trench:

having a spacer composed of a dielectric material upon the oxide layer in contact with the first layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer filling the isolation trench and extending above the oxide layer in contact with the spacer, wherein filling is performed by depositing the second layer, and the depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first layer so as to define an upper surface contour of the second layer; and

having a planar upper surface formed from the second layer and the spacer and being situated above the oxide layer, wherein the planar upper surface is formed by substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the second layer to a planarizing process; and

fusing the oxide layer, electrically insulative material, spacer and second layer;

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

39. (Previously presented) The method as defined in Claim 38, further comprising:
doping the semiconductor substrate with a dopant having a first conductivity type; and
doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of the isolation trenches.

40. (Previously presented) The method as defined in Claim 39, wherein:
the doped trench bottom has a width;
each isolation trench has a width; and
the width of each doped trench bottom is greater than the width of the respective isolation trench.

41. (Cancelled)

42. (Currently amended) A method for forming a microelectronic structure, the method comprising:
providing a semiconductor substrate having a top surface with an oxide layer thereon;
forming a polysilicon layer upon the oxide layer;
forming a first layer upon the polysilicon layer;
forming a first isolation structure including:
a first spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;
a first isolation trench extending from an opening thereto at top edges at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and
a second spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is curved; and

a second spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

rounding the top edges of the isolation trenches;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers of the respective first and second isolation structures, wherein filling is performed by depositing the conformal second layer, and depositing is carried out to ~~the~~ an extent of filling each of the isolation trenches and extending over the spacers and over the first layer so as to define an upper surface contour of the conformal second layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the second layer to a planarizing process;

forming a planar upper surface from the conformal second layer and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide layer; and

fusing the oxide layer, first spacer, second spacer and conformal second layer of the first isolation structure and fusing the oxide layer, first spacer, second spacer and conformal second layer of the second isolation structure;

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

43. (Currently amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon the oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench extending below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers of the respective first and second isolation structures, wherein filling is performed by depositing the conformal second layer, and depositing is carried out to the extent of filling each of the isolation trenches and extending over the spacers and over the first layer so as to define an upper surface contour of the conformal second layer;

substantially simultaneously subjecting ~~the~~ an entire upper surface contour of the second layer to a planarizing process and planarizing the conformal second layer and the first and second spacers of the respective first and second isolation structures to form a planar upper surface from the conformal second layer and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches; and

fusing the oxide layer, first spacer, second spacer and conformal second layer of the first isolation structure and fusing the oxide layer, first spacer, second spacer and conformal second layer of the second isolation structure.

IN THE DRAWINGS:

The attached sheets of drawings include corrections to FIGs. 5B, 7B, 8B, 9A and 9B. These sheets, which include FIGs. 5A, 7A, and 8A, replace the original sheets including FIGs. 5A, 5B, 7A, 7B, 8A, 8B, 9A and 9B. In addition to the four (4) replacement sheets of the amended drawings, a full set of replacement drawings is included in order to make them a consistent style with one another.

Specifically, FIG. 5B has been revised to change one occurrence of reference numeral "22" to --28-- to eliminate redundancy with previously used reference numerals; FIG. 7B has been revised to add three occurrences of the reference numeral --28-- with appropriate lead lines; FIG. 8B has been revised to add six occurrences of the reference numeral --28-- with appropriate lead lines; and FIG. 9B has been revised to add three occurrences of the reference numeral --54-- with brackets and to change the location of reference numerals --64-- to allow insertion of reference numeral --54--. No new matter has been added.

REMARKS

No new matter has been added. The amendments to the specification, claims, and drawings correct typographical errors, improve antecedent basis, and do not affect the scope of the claims. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required.

Respectfully submitted,

Katherine A. Hamer

Katherine A. Hamer
Registration No. 47,628
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: April 23, 2010
KAH/csw

Enclosures: Replacement Sheets (full set)
Annotated Sheets Showing Changes (4)

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EXHIBIT C

(CLAIMS IN ISSUED PATENT)

(Patent No. 7,749,860 B2)

film **36**. As such, a final isolation structure **48** illustrated in FIG. **9**A is achieved. Pad oxide **14** acts as an etch stop for this etch recipe. A residual depression of isolation film **36** may appear centered over filled isolation trench **32**. A depression would be created, centered above isolation trench **32**, during the filling of isolation trench **32** with isolation film **36**, as seen in FIG. **6**A. Where a depression is not detrimental to the final isolation structure **48** as illustrated in FIG. **9**A, this selective etch recipe alternative may be used.

Semiconductor structure **10**, as illustrated in FIG. **9**A, can be seen to have a substantially continuous isolation structure substantially covering semiconductor substrate **12**. An upper surface **42***a* of isolation structure **48** includes the head portion or nail head **54**. Semiconductor substrate **12** is covered at an upper surface **42***b* by either a pad oxide layer or a gate oxide layer. Another upper surface **42***c* comprises the upper surface of the pad oxide layer or gate oxide layer.

A starting structure for an example of a second embodiment of the present invention is illustrated in FIG. **2**B. In FIG. **2**B, pad oxide **14** is grown upon semiconductor substrate **12** and a polysilicon layer **18** is deposited upon pad oxide **14**. This embodiment of the present invention parallels the processing steps of the first embodiment with the additional processing that takes into account the use of polysilicon layer **18**.

FIG. **3**B illustrates etching through nitride layer **16** and polysilicon layer **18** to stop on pad oxide **14**. The etch creates both an insulator island **22** and a polysilicon island **24** formed, respectively, from nitride layer **16** and polysilicon layer **18**.

FIG. **4**B illustrates further processing of the structure depicted in FIG. **3**B, wherein insulation film **26** has been deposited upon insulator island **22**, laterally exposed portions of polysilicon island **24**, and exposed portions of pad oxide **14**. Following deposition of insulation film **26**, a spacer etch and an isolation trench etch are carried out similarly to the spacer etch and isolation trench etch carried out upon semiconductor structure **10** illustrated in FIG. **5**A.

FIG. **5**B illustrates the results of both the spacer etch and the isolation trench etch and optional implantation of isolation trench **32** to form trench bottom **34** analogous to doped trench bottom **34** illustrated in FIG. **5**A. Formation of insulation liner **30** within isolation trench **32** preferentially precedes implantation to form P-doped trench bottom **34**. Following optional implantation of doping ions, full or partial removal of spacer **28** may optionally be performed as set forth above with respect to the first embodiment of the invention.

FIG. **6**B illustrates a subsequent step in fabrication of an isolation trench according to the second embodiment of the inventive method, wherein isolation film **36** is deposited both within isolation trench **32**, and over both of insulator island **22** and spacer **28**. As set forth above, densification of isolation film **36** is a preferred step to be carried out either at this stage of fabrication or at a subsequent selective stage. Planarization or etchback of isolation film **36** is next carried out as set forth in the first embodiment of the present invention, and as illustrated in FIG. **7**B.

The process of planarization or etchback of isolation film **36** reduces insulator island **22** to form reduced island **52** as illustrated in FIG. **7**B. Next, additional selective ion implantations can be made through polysilicon island **24** and into the active area of semiconductor substrate **12** that lies beneath polysilicon island **24**.

In FIG. **8**B, it can be seen in phantom that spacer **28** has a top surface that is co-planar with third upper surface **42** of isolation structure **48** after planarization. Polysilicon island **24** an spacer **28** are formed as shown in FIG. **8**B. Removal of spacer **28** from the structures illustrated in FIG. **8**B can be accomplished by patterning and etching with a mask that covers head **54** that extends above and away from isolation trench **32** seen in FIG. **8**B. The etching process exposes a surface on semiconductor substrate **12** upon which a gate oxide layer is deposited or grown.

To form the structure seen in FIG. **9**B, semiconductor structures **10** of FIGS. **7**B or **8**B are subjected to implantation of semiconductor substrate **12** with ions. Semiconductor structure **10** is then subjected to a heat treatment so as to fuse together isolation film **36**, optional pad oxide **14**, insulation liner **30**, and spacer **28** into an integral filled isolation trench.

Subsequent to the process illustrated in FIGS. **6**A-**8**A and **6**B-**9**B a final thermal treatment, or subsequent thermal treatments, can be performed. Heat treatment may cause isolation structure **48** to be wider proximal to third upper surface **42** than proximal to doped trench bottom **34**. When so shaped, an unoxidized portion of the active area of semiconductor substrate **12** that forms sidewall **50** would have a trapezoidal shape when viewed in cross-section, where the widest portion is second upper surface **40** and the narrowest portion is at doped trench bottom **34**. Where a trapezoidal shape of the trench portion causes unwanted encroachment into the active area of semiconductor substrate **12**, the optional formation of insulation liner **30** from a nitride material or equivalent is used to act as an oxidation barrier for sidewall **50**. Semiconductor structure **10** is illustrated in FIG. **9**B as being implanted by doping ions, as depicted with downwardly directed arrows. Following a preferred implantation, thermal processing may be carried out in order to achieve dopant diffusion near upper surface **42***b* of implanted ions residing within semiconductor substrate **12**. Due to head **54** extending onto semiconductor substrate **12**, a doping concentration gradient can be seen between the active area **53***a* and the active area **53***b*. The starting and stopping point of the doping concentration gradient in relation to flange sidewalls **64** will depend upon the duration and temperature of a thermal treatment.

The present invention may be carried out wherein spacer **28** and isolation film **36** are substantially composed of the same oxide material, and insulator island **22** is substantially composed of a nitride composition. Other compositions may be chosen wherein etch selectivity or CMP selectivity slightly favors insulator island **22** over both spacer **28** and isolation film **36**. The specific selection of materials will depend upon the application during fabrication of the desired isolation trench.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrated and not restrictive. The scope of the invention is, therefore, indicated by the appended claims and their combination in whole or in part rather than by the foregoing description. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured by United States Letters Patent is:

1. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon the oxide layer;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer over the oxide layer and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer over and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer into the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

forming a liner upon a sidewall of each isolation trench;

filling each isolation trench with a conformal layer, the conformal layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein the filling is performed by depositing the conformal layer, and the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal layer;

substantially simultaneously subjecting the entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal layer at least to the first dielectric layer and each spacer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

fusing the oxide layer, liner, spacers and conformal layer;

wherein the conformal layer comprises a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches.

2. The method according to claim 1, wherein forming a liner upon a sidewall of each isolation trench comprises thermally growing oxide on the semiconductor substrate.

3. The method according to claim 1, wherein forming the liner upon the sidewall of the isolation trench comprises depositing a composition of matter.

4. The method according to claim 1, further comprising forming a doped region below the termination of each isolation trench within the semiconductor substrate.

5. The method according to claim 1, wherein the upper surface for each isolation trench is formed by chemical-mechanical planarization.

6. A method of forming a microelectronic structure, the method comprising:

forming a first dielectric layer upon an oxide layer over a semiconductor substrate;

selectively removing the first dielectric layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer over the oxide layer and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer into the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has an edge;

rounding a top edge of each of the plurality of isolation trenches;

filling each isolation trench with a conformal layer, the conformal layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal layer and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal layer;

substantially simultaneously subjecting an entire upper surface contour of the conformal layer to a planarizing process and planarizing the conformal layer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

fusing the oxide layer, spacers and conformal layer;

wherein:

the conformal layer comprises a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches;

the conformal layer and the spacers form the upper surface for each isolation trench, each upper surface being formed from the conformal layer and the spacers and being situated above the oxide layer; and

the first dielectric layer is in contact with at least a pair of the spacers and the oxide layer.

7. The method according to claim 6, further comprising:

forming a gate oxide upon the semiconductor substrate.

8. The method according to claim 6, wherein removing portions of the conformal material comprises etching the material using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range from about 1:1 to about 2:1.

9. The method according to claim 8, wherein etching the material using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range from about 1:1 to about 2:1 comprises etching the conformal material the ratio is in a range from about 1.3:1 to about 1.7:1.

10. The method according to claim 6, wherein removing portions of the conformal material overlying the remaining portions of the oxide comprises:

chemical mechanical planarization, wherein the conformal material, the spacers, and the first dielectric material form a planar first upper surface; and

etching to form a second upper surface situated above the oxide.

11. The method according to claim 6, wherein removing portions of the conformal material that overlie the remaining portions of the oxide further comprises etching using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range of from about 1:1 to about 2:1.

12. The method according to claim 11, wherein etching using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range from about 1:1 to about 2:1 comprises etching using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range of from about 1.3:1 to about 1.7:1.

13. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon the oxide layer;

selectively removing the silicon nitride layer to expose the oxide layer at a plurality of areas;

forming a first silicon dioxide layer over the oxide layer and over the silicon nitride layer, wherein forming a first silicon dioxide layer includes forming a first silicon

dioxide layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer to form a plurality of spacers from the first silicon dioxide layer, wherein each spacer is situated upon the oxide layer, is in contact with the silicon nitride layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer into and terminating within the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

forming a corresponding electrically active region below the termination of each isolation trench within the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer to the termination of the isolation trench within the semiconductor substrate;

filling each isolation trench with a conformal second silicon dioxide layer, the conformal second silicon dioxide layer within each isolation trench extending above the oxide layer in contact with the corresponding pair of the spacers, wherein filling is performed by depositing the conformal second silicon dioxide layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and the silicon nitride layer so as to define an upper surface contour of the conformal second silicon dioxide layer;

substantially simultaneously subjecting an entire upper surface contour of the conformal second silicon dioxide layer to a planarizing process so as to remove the conformal second silicon dioxide layer and the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above the oxide layer, wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

fusing the oxide layer, liner, spacers and conformal second silicon dioxide layer.

14. The method according to claim **13**, wherein forming a liner upon a sidewall of each isolation trench comprises forming a thermally grown oxide upon a sidewall of the semiconductor substrate.

15. The method according to claim **13**, wherein forming a liner upon a sidewall of each isolation trench comprises forming a liner composed of silicon nitride.

16. The method according to claim **14**, further comprising: forming a gate oxide upon the semiconductor substrate.

17. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over the oxide layer, the polysilicon layer, and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer is upon the oxide layer, is in contact with both the polysilicon layer and the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

rounding the top edges of each of the isolation trenches;

filling each isolation trench with a conformal third layer, the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal third layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal third layer;

substantially simultaneously subjecting an entire upper surface contour of the conformal third layer to a planarizing process and planarizing the conformal third layer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

fusing the oxide layer, spacers and conformal third layer;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

18. The method according to claim **17**, wherein the upper surface for each isolation trench is formed by chemical-mechanical planarization.

19. The method according to claim **17**, wherein implanting comprises forming a doped region below the termination of each isolation trench within the semiconductor substrate.

20. The method according to claim **17**, wherein rounding the top edges of each of the isolation trenches comprises forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third material is electrically insulative.

21. The method according to claim **20**, wherein forming a liner upon a sidewall of each isolation trench comprises forming a thermally grown oxide upon a sidewall the semiconductor substrate.

22. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over the oxide layer, the polysilicon layer, and the first dielectric layer, wherein forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer is upon the oxide layer, is in contact with both the polysilicon layer and the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

rounding the top edges of each isolation trench of the plurality of isolation trenches;

filling each isolation trench of the plurality of isolation trenches with a conformal third layer, the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal third layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal third layer;

substantially simultaneously subjecting an entire upper surface contour of the conformal third layer to a planarizing process and planarizing the conformal third layer to form therefrom an upper surface for each isolation trench of the plurality of isolation trenches that is co-planar to the other upper surfaces; and fusing the oxide layer, spacers and conformal third layer;

wherein the conformal third layer is an electrically insulative material that extends continuously between and within the plurality of isolation trenches;

wherein the upper surface for each isolation trench of the plurality of isolation trenches is formed from the conformal third layer, the spacers, and the first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

23. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over the oxide layer, the polysilicon layer, and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer of the plurality of spacers is upon the oxide layer, is in contact with both the polysilicon layer and the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

rounding the top edges of each of the isolation trenches;

filling each isolation trench with a conformal third layer, the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal third layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal third layer;

substantially simultaneously subjecting an entire upper surface contour of the conformal third layer to a planarizing process and planarizing the conformal third layer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces;

exposing the oxide layer upon a portion of a surface of the semiconductor substrate;

forming a gate oxide layer upon the portion of the surface of the semiconductor substrate;

forming between the plurality of isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with a pair of the spacers;

selectively removing the third layer, the spacers, and the layer composed of polysilicon to form a portion of at least one of the upper surfaces; and

fusing the oxide layer, spacers and conformal third layer;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

24. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over the oxide layer, the polysilicon layer, and the first dielectric layer, wherein the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at the plurality of areas;

selectively removing the second dielectric layer to form a plurality of spacers from the second dielectric layer, wherein each spacer of the plurality of spacers is upon the oxide layer, is in contact with both the polysilicon layer and the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

rounding the top edges of each isolation trench of the plurality of isolation trenches;

filling each isolation trench with a conformal third layer, the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal third layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer so as to define an upper surface contour of the conformal third layer;

substantially simultaneously subjecting an entire upper surface contour of the conformal third layer to a planarizing process comprising an etch recipe that etches the conformal third layer and the spacers faster than the first dielectric by a ratio in a range from about 1:1 to about 2:1 and planarizing the conformal third layer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

fusing the oxide layer, spacers and conformal third layer;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches. corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric material so as to define an upper surface contour of the conformal third material;

25. The method according to claim 24, wherein the ratio is in a range from about 1.3:1 to about 1.7:1.

26. A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the pad oxide layer;

forming a silicon nitride layer upon the polysilicon layer;

selectively removing the silicon nitride layer and the polysilicon layer to expose the pad oxide layer at a plurality of areas;

forming a first silicon dioxide layer over the pad oxide layer and over the silicon nitride layer, wherein the forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed pad oxide layer at the plurality of areas;

selectively removing the first silicon dioxide layer to form a plurality of spacers from the first silicon dioxide layer, wherein each spacer of the plurality of spacers is situated upon the pad oxide layer, is in contact with the silicon nitride layer and the polysilicon layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches extending below the pad oxide layer and from top edges into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

forming a corresponding doped region below the termination of each isolation trench within the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench, each liner extending from an interface thereof with the pad oxide layer to the termination of the isolation trench within the semiconductor substrate;

rounding the top edges of the isolation trenches;

filling each isolation trench with a conformal second layer, the conformal second layer extending above the pad oxide layer in contact with a corresponding pair of the spacers, wherein filling is performed by depositing the conformal second layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the silicon nitride layer so as to define an upper surface contour of the conformal second layer;

substantially simultaneously subjecting an entire upper surface contour of the conformal second layer to a planarizing process and planarizing the conformal second layer and each of the spacers to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces and is situated above the pad oxide layer; and

fusing the pad oxide layer, liner, spacers and conformal second layer;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

27. The method according to claim 26, wherein each liner is a thermally grown oxide of the semiconductor substrate, and wherein the conformal second material is electrically insulative.

28. The method according to claim 26, wherein each liner is composed of silicon nitride, and wherein the conformal second material is electrically insulative.

29. The method according to claim 26, further comprising:

exposing the pad layer upon a portion of a surface of the semiconductor substrate;

forming a gate oxide layer upon the portion of the surface of the semiconductor substrate;

forming between the plurality of isolation trenches, and confined in a space therebetween, a layer composed of polysilicon upon the gate oxide layer in contact with a pair of the spacers, and

selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surfaces.

30. A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer;

forming a first layer upon the polysilicon layer;

selectively removing the first layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the exposed oxide layer at the plurality of areas, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches, each isolation trench:

having a spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer filling the isolation trench and extending above the oxide layer in contact with the spacer, wherein filling is performed by depositing the second layer, and depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first layer so as to define an upper surface contour of the second layer; and

having a planar upper surface formed from the second layer and the spacer and being situated above the oxide layer, wherein the planar upper surface is formed by substantially simultaneously subjecting an entire upper surface contour of the second layer to a planarizing process; and

fusing the oxide layer, spacer and second layer;

wherein the microelectronic structure is defined at least in part by a plurality of spacers, the second layer, and the plurality of isolation trenches.

31. The method as defined in claim 30, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one isolation trench of the plurality of isolation trenches.

32. The method according to claim 31, wherein the doped trench bottom has a width, each isolation trench has a width,

and the width of each doped trench bottom is greater than the width of the respective isolation trench.

33. A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon the oxide layer;

selectively removing the first layer to expose the oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the oxide layer at the plurality of areas, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches without filling the plurality of isolation trenches, each isolation trench:

having a spacer composed of a dielectric material upon the oxide layer in contact with the first layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer filling the isolation trench and extending above the oxide layer in contact with the spacer, wherein filling is performed by depositing the second layer, and the depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first layer so as to define an upper surface contour of the second layer; and

having a planar upper surface formed from the second layer and the spacer and being situated above the oxide layer, wherein the planar upper surface is formed by substantially simultaneously subjecting an entire upper surface contour of the second layer to a planarizing process; and

fusing the oxide layer, electrically insulative material, spacer and second layer;

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

34. The method according to claim 33, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type;

and wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide further comprises;

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of the isolation trenches.

35. The method of claim 34, wherein:

the doped trench bottom has a width;

each isolation trench has a width; and

the width of each doped trench bottom is greater than the width of the respective isolation trench.

36. A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon the oxide layer;

forming a first layer upon the polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is curved; and

a second spacer composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

rounding the top edges of the isolation trenches;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers of the respective first and second isolation structures, wherein filling is performed by depositing the conformal second layer, and depositing is carried out to an extent of filling each of the isolation trenches and extending over the spacers and over the first layer so as to define an upper surface contour of the conformal second layer;

substantially simultaneously subjecting an entire upper surface contour of the second layer to a planarizing process;

forming a planar upper surface from the conformal second layer and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide layer; and

fusing the oxide layer, first spacer, second spacer and conformal second layer of the first isolation structure and fusing the oxide layer, first spacer, second spacer and conformal second layer of the second isolation structure;

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

37. A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon the oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench extending below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers of the respective first and second isolation structures, wherein filling is performed by depositing the conformal second layer, and depositing is carried out to the extent of filling each of the isolation trenches and extending over the spacers and over the first layer so as to define an upper surface contour of the conformal second layer;

substantially simultaneously subjecting an entire upper surface contour of the second layer to a planarizing process and planarizing the conformal second layer and the first and second spacers of the respective first and second isolation structures to form a planar upper surface from the conformal second layer and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches; and

fusing the oxide layer, first spacer, second spacer and conformal second layer of the first isolation structure and fusing the oxide layer, first spacer, second spacer and conformal second layer of the second isolation structure.

* * * * *

EXHIBIT D

(CLEAN CLAIMS INCLUDING CERTIFICATE OF CORRECTION CHANGES)

(Patent No. 7,749,860 B2)

1. A method of forming a microelectronic structure, the method comprising:

forming a first dielectric material upon an oxide over a semiconductor substrate;

selectively removing the first dielectric material to expose a plurality of areas of the oxide;

forming a second dielectric material over the first dielectric material and in contact with the plurality of exposed areas of the oxide;

selectively removing the second dielectric material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide in contact with lateral edges of the first dielectric material;

removing a portion of material from the plurality of areas of the oxide at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench of the plurality of isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;

depositing a conformal material in each isolation trench, the conformal material extending over remaining portions of the oxide in contact with a corresponding pair of the spacers, wherein the depositing is performed to the extent of filling each isolation trench and extending over the spacers and over the first dielectric material so as to define an upper surface contour of the conformal material;

removing portions of the conformal material overlying the remaining portions of the oxide by planarizing the conformal material at least to the first dielectric material and each spacer such that an upper surface for each isolation trench t is co-planar to the other upper surfaces;

the conformal material comprising a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches; and

removing the first dielectric material and portions of the oxide underlying the first dielectric material such that the conformal material fills each said isolation trench, extends horizontally away from each said isolation trench upon remaining portions of the oxide and sidewalls of the conformal material start on an upper surface of the semiconductor substrate and are substantially orthogonal to the upper surface contour of the conformal material.

2. The method according to Claim 1, wherein forming a liner upon a sidewall of each isolation trench comprises thermally growing oxide on the semiconductor substrate.

3. The method according to Claim 1, wherein forming the liner upon a sidewall of each isolation trench comprises depositing a composition of matter.

4. The method according to Claim 1, wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide comprises forming a doped region below the termination of each of said plurality of the isolation trenches within the semiconductor substrate.

5. The method according to Claim 1, wherein removing portions of the conformal material overlying the remaining portions of the oxide comprises removing portions of the conformal material overlying the remaining portions of the oxide by chemical-mechanical planarization.

6. A method of forming a microelectronic structure, the method comprising:
forming a first dielectric material upon an oxide over a semiconductor substrate;
selectively removing the first dielectric material to expose a plurality of areas of the oxide;
forming a second dielectric material over the first dielectric material and in contact with the plurality of exposed areas of the oxide;
selectively removing the second dielectric material to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide in contact with lateral edges of the first dielectric material;
removing a portion material from the plurality of areas of the oxide at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into the semiconductor substrate;
rounding a top edge of each of the plurality of isolation trenches;
implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;

depositing a conformal material filling each isolation trench, the conformal material extending over remaining portions of the oxide in contact with a corresponding pair of the spacers, wherein the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric material so as to define an upper surface contour of the conformal material;

removing portions of the conformal material that overlie the remaining portions of the oxide by a planarizing the conformal material to form an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

removing the first dielectric material and portions of the oxide underlying the first dielectric material such that the conformal material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal material begin on an upper surface of the semiconductor substrate and are oriented substantially orthogonal to the upper surface contour of the conformal material

wherein:

the conformal material is electrically insulative and extends continuously between and within the plurality of isolation trenches;

the conformal material and the spacers form the upper surface for each isolation trench, each upper surface being formed from the conformal material and the spacers and being situated above the oxide; and

the first dielectric material is in contact with at least a pair of the spacers and the oxide .

7. The method according to Claim 6, further comprising:

forming a gate oxide upon the semiconductor substrate.

8. The method according to Claim 6, wherein removing portions of the conformal material comprises etching the material using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range from about 1:1 to about 2:1.

9. The method according to Claim 8, wherein etching the material using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range from about 1:1 to about 2:1 comprises etching the conformal material using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range of from about 1.3:1 to about 1.7:1.

10. The method according to Claim 6, wherein removing portions of the conformal material that overlie the remaining portions of the oxide comprises:

chemical-mechanical planarization, wherein the conformal material, the spacers, and the first dielectric material form a planar first upper surface; and

etching to form a second upper surface situated above the oxide .

11. The method according to Claim 6, wherein removing portions of the conformal material that overlie the remaining portions of the oxide further comprises etching using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range of from about 1:1 to about 2:1.

12. The method according to Claim 11, wherein etching using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range from about 1:1 to about 2:1 comprises etching using an etch recipe that etches the conformal material faster than the first dielectric material by a ratio in a range of from about 1.3:1 to about 1.7:1.

13. A method of forming a microelectronic structure, the method comprising:

forming an oxide upon a semiconductor substrate;

forming a silicon nitride upon the oxide;

selectively removing the silicon nitride to expose a plurality of areas of the oxide;

forming a first silicon dioxide material over the silicon nitride and in contact with the plurality of exposed areas of the oxide;

selectively removing the first silicon dioxide material to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide in contact with lateral edges of the silicon nitride;

removing a portion of material from the plurality of areas at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into the semiconductor substrate,;

forming a corresponding electrically active region below the termination of each isolation trench within the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;

depositing a conformal second silicon dioxide material filling each isolation trench and extending over the remaining portions of the oxide in contact with the corresponding pair of the spacers, the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and the silicon nitride so as to define an upper surface contour of the conformal second silicon dioxide material;

removing portions of the conformal second silicon dioxide material and the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches; and

removing the silicon nitride and portions of the oxide underlying the silicon nitride such that the conformal second silicon dioxide material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second silicon dioxide material start on an upper surface of the semiconductor substrate and lie substantially orthogonal to the upper surface contour of the second silicon dioxide material.

14. The method according to Claim 13, wherein forming a liner upon a sidewall of each isolation trench comprises forming a thermally grown oxide upon a sidewall of the semiconductor substrate.

15. The method according to Claim 13, wherein forming a liner upon a sidewall of each isolation trench comprises forming a liner composed of silicon nitride.

16. The method according to Claim 14, further comprising:

forming a gate oxide upon the semiconductor substrate.

17. A method of forming a microelectronic structure, the method comprising:

forming an oxide upon a semiconductor substrate;

forming polysilicon upon the oxide;

forming a first dielectric material upon the polysilicon;

selectively removing the first dielectric material and the polysilicon to expose a plurality of areas of the oxide;

forming a second dielectric material conformally over the polysilicon, the first dielectric material and in contact with the plurality of exposed areas of the oxide;

selectively removing the second dielectric material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide in contact with lateral edges of the first dielectric material;

removing a portion of material from the plurality of areas of the oxide at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

rounding the top edges of each of the isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;

depositing a conformal third material filling each isolation trench the conformal third material extending over remaining portions of the oxide in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric material so as to define an upper surface contour of the conformal third material;

removing portions of the conformal third material by planarizing the conformal third material to form an upper surface for each isolation trench that is co-planar to the other upper surfaces; and

removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the

oxide and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches.

18. The method according to Claim 17, wherein removing portions of the conformal third material comprises removing portions of the conformal third material by chemical-mechanical planarization.

19. The method according to Claim 17, wherein implanting comprises forming a doped region below the termination of each isolation trench within the semiconductor substrate.

20. The method according to Claim 17, wherein rounding the top edges of each of the isolation trenches comprises forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third material is of an electrically insulative.

21. The method according to Claim 20, wherein forming a liner upon a sidewall of each isolation trench comprises forming a thermally grown oxide upon a sidewall of the semiconductor substrate.

22. A method of forming a microelectronic structure, the method comprising:

forming an oxide upon a semiconductor substrate;

forming polysilicon upon the oxide;

forming a first dielectric material upon the polysilicon;

selectively removing the first dielectric material and the polysilicon to expose plurality of areas of the oxide;

forming a second dielectric material over the polysilicon, the first dielectric material and in contact with the plurality of exposed areas of the oxide;

selectively removing the second dielectric material to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide in contact with lateral edges of the first dielectric material;

removing a portion of material from the plurality of exposed areas of the oxide at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;

depositing a conformal third material filling each isolation trench, the conformal third material extending over remaining portions of the oxide in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric material so as to define an upper surface contour of the conformal third material;

removing portions of the conformal third material by planarizing the conformal third material to form an upper surface for each isolation trench of the plurality of isolation trenches that is co-planar to the other upper surfaces;

removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material;

wherein the conformal third material is electrically insulative and extends continuously between and within the plurality of isolation trenches;

wherein the upper surface for each isolation trench of the plurality of isolation trenches is formed from the conformal third material, the spacers, and the first dielectric material; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches.

23. A method of forming a microelectronic structure, the method comprising:

forming an oxide upon a semiconductor substrate;

forming a first polysilicon material upon the oxide;

forming a first dielectric material upon the first polysilicon material;

selectively removing the first dielectric material and the first polysilicon material to expose a plurality of areas of the oxide;

forming a second dielectric material over the first dielectric material and in contact with the plurality of exposed areas of the oxide;

selectively removing the second dielectric material to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide in contact with lateral edges of the first dielectric material;

removing a portion of material from the plurality of exposed areas of the oxide at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

rounding the top edges of each of the isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;

depositing a conformal third material filling each isolation trench, the conformal third material extending over remaining portions of the oxide in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric material so as to define an upper surface contour of the conformal third material;

removing portions of the conformal third material overlying the remaining portions of the oxide by planarizing the conformal third material to form an upper surface for each isolation trench that is co-planar to the other upper surfaces;

exposing the oxide upon a portion of a surface of the semiconductor substrate;

forming a gate oxide upon the portion of the surface of the semiconductor substrate;

forming between the plurality of isolation trenches, and confined in the space therebetween, a second polysilicon material upon the oxide in contact with a pair of the spacers;

selectively removing the conformal third material, the spacers, and the second polysilicon material to form a portion of at least one of the upper surfaces; and

removing the first dielectric material, first polysilicon material and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate and extend to the upper surface contour of the conformal third material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

24. A method of forming a microelectronic structure, the method comprising:

forming polysilicon upon an oxide overlying a semiconductor substrate;

forming a first dielectric material upon the polysilicon;

selectively removing the first dielectric material and the polysilicon to expose a plurality of areas of the oxide;

forming a second dielectric material over the polysilicon, the first dielectric material and in contact with the plurality of exposed areas of the oxide;

selectively removing the second dielectric material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide in contact with lateral edges of the first dielectric material;

removing material from the plurality of exposed areas of the oxide at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

rounding the top edges of each isolation trench of the plurality of isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;

depositing a conformal third material filling each isolation trench, with a conformal third layer, the conformal third layer extending over remaining portions of the oxide in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric material so as to define an upper surface contour of the conformal third material;

removing portions of the conformal third material overlying the remaining portions of the oxide by planarizing the conformal third material to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces using an etch recipe that etches the conformal third material and the spacers faster than the first dielectric material by a ratio in a range of from about 1:1 to about 2:1; and

heat treating the oxide, spacers and conformal third material to fuse the oxide, spacers and conformal third material; and

removing the first dielectric material, polysilicon and portions of the oxide underlying the first dielectric material such that the conformal third material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third material, and the plurality of isolation trenches.

25. The method according to Claim 24, wherein the ratio is in a range from about 1.3:1 to about 1.7:1.

26. A method of forming a microelectronic structure, the method comprising:

forming a pad oxide upon a semiconductor substrate;

forming a first polysilicon material upon the pad oxide;

forming silicon nitride upon the first polysilicon material;

selectively removing the silicon nitride and the first polysilicon material to expose a plurality of areas of the pad oxide material;

forming a first silicon dioxide material over the silicon nitride and in contact with the exposed pad oxide at the plurality of exposed areas of the pad oxide;

selectively removing the first silicon dioxide material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the pad oxide in contact with lateral edges of the silicon nitride and the first polysilicon material;

removing a portion of material from the plurality of exposed areas at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

forming a corresponding doped region below the termination of each isolation trench within the semiconductor substrate by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the pad oxide;

forming a liner upon a sidewall of each isolation trench, each liner extending from an interface thereof with the pad oxide to the termination of the isolation trench within the semiconductor substrate;

rounding the top edges of the isolation trenches;

depositing a conformal second material filling each isolation trench, the conformal second material extending over remaining portions of the pad oxide in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the silicon nitride so as to define an upper surface contour of the conformal second material;

removing a portion of the conformal second material by planarizing the conformal second material and each of the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and is situated above the pad oxide;

heat treating the pad oxide, liner, spacers and conformal second material to fuse the pad oxide, liner, spacers and conformal second material; and

removing the silicon nitride, first polysilicon material and portions of the pad oxide underlying the silicon nitride such that the conformal second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the pad oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and continue to the upper surface contour of the conformal second material, the sidewalls lie substantially orthogonal to the upper surface contour of the conformal second material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

27. The method according to Claim 26, wherein each liner is a thermally grown oxide of the semiconductor substrate, and wherein the conformal second material is electrically insulative.

28. The method according to Claim 26, wherein each liner is composed of silicon nitride, and wherein the conformal second material is electrically insulative.

29. The method according to Claim 26, further comprising:

forming a gate oxide upon a portion of the surface of the semiconductor substrate;

forming between the plurality of isolation trenches, and confined in a space therebetween, a second polysilicon material upon the gate oxide in contact with a pair of the spacers, and

selectively removing the second polysilicon material to form a portion of at least one of the upper surfaces.

30. A method for forming a microelectronic structure, the method comprising:

forming polysilicon upon an oxide overlying a semiconductor substrate;

forming a first material upon the polysilicon;

selectively removing the first material and the polysilicon to expose a plurality of areas of the oxide;

forming a plurality of isolation trenches through the exposed oxide at the plurality of areas;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide;

wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches, each isolation trench:

having a spacer composed of a dielectric material upon the oxide in contact with the first material and the polysilicon;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second material filling the isolation trench and extending above the oxide in contact with the spacer, wherein filling is performed by depositing the second material, and depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first material so as to define an upper surface contour of the second material; and

having a planar upper surface formed from the second material and the spacer and being situated above the oxide, wherein the planar upper surface is formed by substantially simultaneously subjecting an entire upper surface contour of the second material to a planarizing process; and

removing the first material, polysilicon and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and end at the upper surface contour of the second material, the sidewalls are substantially orthogonal to the upper surface contour of the second material;

wherein the microelectronic structure is defined at least in part by a plurality of spacers, the second material, and the plurality of isolation trenches.

31. The method according to Claim 30, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide further comprises:

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one isolation trench of the plurality of isolation trenches.

32. The method according to Claim 31, wherein the doped trench bottom has a width, each isolation trench has a width, and the width of each doped trench bottom is greater than the width of the respective isolation trench.

33. A method for forming a microelectronic structure, the method comprising:

forming a first material upon an oxide overlying a semiconductor substrate;

selectively removing the first material to expose a plurality of areas of the oxide;

forming a plurality of isolation trenches through the oxide at the plurality of areas, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches without filling the plurality of isolation trenches, each isolation trench:

having a spacer composed of a dielectric material upon the oxide in contact with the first material;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second material filling the isolation trench and extending above the oxide in contact with the spacer, wherein filling is performed by depositing the second material, and the depositing is carried out to the extent of filling each isolation trench and extending over the spacer and over the first material so as to define an upper surface contour of the second material; and

having a planar upper surface formed from the second material and the spacer and being situated above the oxide, wherein the planar upper surface is formed by removing portions of the second material by planarizing the entire upper surface contour of the second material;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide; and

removing the first material and portions of the oxide underlying the first material such that the second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material commence at an upper surface of the semiconductor substrate and end at the upper surface contour of the second material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material;

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second material, and the plurality of isolation trenches.

34. The method according to Claim 33, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide further comprises:

doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of the isolation trenches.

35. The method according to Claim 34, wherein:

the doped trench bottom has a width;

each isolation trench has a width; and

the width of each doped trench bottom is greater than the width of the respective isolation trench.

36. A method for forming a microelectronic structure, the method comprising:

forming polysilicon upon an oxide overlying a semiconductor substrate;

forming a first material upon the polysilicon

forming a first isolation structure including:

a first spacer composed of a dielectric material upon the oxide in contact with the first material and the polysilicon;

a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide in contact with the first material and the polysilicon, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon the oxide in contact with the first material and the polysilicon;

a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is curved; and

a second spacer composed of a dielectric material upon the oxide in contact with the first material and the polysilicon, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

rounding the top edges of the isolation trenches;

doping the first isolation trench and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

depositing a conformal second material comprising an electrically insulative material, the conformal second material filling the first and second isolation trenches and extending continuously over remaining portions of the oxide in contact with the first and second spacers of the respective first and second isolation structures, wherein depositing is carried out to an extent of filling each of the isolation trenches and extending over the spacers and over the first material so as to define an upper surface contour of the conformal second material;

planarizing portions of the upper surface contour of the second material;

forming a planar upper surface from the conformal second material and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide;

heat treating the oxide, first spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure;

heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure; and

removing the first material, polysilicon and portions of the oxide underlying the first material such that the conformal second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material;

wherein the microelectronic structure is defined at least in part by the active area, the second material, and the first and second isolation trenches.

37. A method for forming a microelectronic structure, the method comprising:

forming a first material upon an oxide overlying a semiconductor substrate;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon the oxide in contact with the first material;

a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide material in contact with the first material, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon the oxide material in contact with the first material;

a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is rounded; and

a second spacer composed of a dielectric material upon the oxide in contact with the first material, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

doping the first isolation trench and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

depositing a conformal second material comprising an electrically insulative material to fill the first and second isolation trenches and extending continuously over remaining portions of the oxide in contact with the first and second spacers of the respective first and second isolation structures, wherein the depositing is carried out to the extent of filling each of the isolation trenches and extending over the spacers and over the first material so as to define an upper surface contour of the conformal second material;

planarizing the conformal second material and the first and second spacers of the respective first and second isolation structures to form a planar upper surface;

heat treating the oxide, first spacer, second spacer and conformal second material of the first isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the first isolation structure;

heat treating the oxide, first spacer, second spacer and conformal second material of the second isolation structure to fuse the oxide, first spacer, second spacer and conformal second material of the second isolation structure; and

removing the first material and portions of the oxide underlying the first material such that the conformal second material fills each isolation trench, extends horizontally away from each isolation trench upon remaining portions of the oxide and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the conformal second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal second material.